HITACHI

SM00025

C28WF523N
C32WF523N
C32WF720N
C32WF727N
C32WF810N
C36WF810N
C36WF830N
CL28WF720AN
CL32WF720AN
CL32WF720AND
CL32WF727N
CL32WF810AN
CL36WF810AN
CL36WF830AN
D36WF840N

SERVICE MANUAL
MANUEL D'ENTRETIEN
WARTUNGSHANDBUCH

CAUTION:

Before servicing this chassis, it is important that the service technician read the "Safety Precautions" and "Product Safety Notices" in this service manual.

ATTENTION:

Avant d'effectuer l'entretien du châassis, le technicien doit lire les «Précautions de sécurité» et les «Notices de sécurité du produit» présentés dans le présent manuel.

VORSICHT:

Vor Öffnen des Gehäuses hat der Service-Ingenieur die „Sicherheitshinweise" und „Hinweise zur Produktsicherheit" in diesem Wartungshandbuch zu lesen.

Data contained within this Service manual is subject to alteration for improvement.

Les données fournies dans le présent manuel d'entretien peuvent faire l'objet de modifications en vue de perfectionner le produit.

Die in diesem Wartungshandbuch enthaltenen Spezifikationen können sich zwecks Verbesserungen ändern.

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

COLOUR TELEVISION
DECEMBER 1999

⚠ SAFETY PRECAUTIONS

WARNING: The following precautions must be observed.

ALL PRODUCTS

Before any service is performed on the chassis an isolation transformer should be inserted between the power line and the product.

When replacing the chassis in the cabinet, ensure all the protective devices are put back in place.

When service is required, observe the original lead dressing. Extra precaution should be taken to ensure correct lead dressing in any high voltage circuitry area.

Many electrical and mechanical parts in HITACHI products have special safety related characteristics. These characteristics are often not evident from visual inspection, nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified by marking with a ⚠ on the schematics and the replacement parts list.
The use of a substitute replacement component that does not have the same safety characteristics as the HITACHI recommended replacement one, shown in the parts list, may create electrical shock, fire, X-radiation, or other hazards.

Always replace original spacers and maintain lead lengths. Furthermore, where a short circuit has occurred, replace those components that indicate evidence of overheating.

Insulation resistance should not be less than 2MΩ at 500V DC between the main poles and any accessible metal parts.

No flashover or breakdown should occur during the dielectric strength test, applying 3KV AC or 4.25KV DC for two seconds between the main poles and accessible metal parts.

Before returning a serviced product to the customer, the service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock. The service technician must make sure that no protective device built into the instrument by the manufacturer has become defective, or inadvertently damaged during servicing.

CE MARK

HITACHI products may contain the CE mark on the rating plate indicating that the product contains parts that have been specifically approved to provide electromagnetic compatibility to designated levels.

When replacing any part in this product, please use only the correct part itemised in the parts list to ensure this standard is maintained, and take care to replace lead dressing to its original state, as this can have a bearing on the electromagnetic radiation/immunity.

PICTURE TUBE

The line output stage can develop voltages in excess of 25KV; if the E.H.T. cap is required to be removed, discharge the anode to chassis via a high value resistor, prior to its removal from the picture tube.

High voltage should always be kept at the rated value of the chassis and no higher. Operating at higher voltages may cause a failure of the picture tube or high voltage supply, and also, under certain circumstances could produce X-radiation levels moderately in excess of design levels. The high voltage must not, under any circumstances, exceed 29KV on the chassis (except for projection Televisions).

The primary source of X-radiation in the product is the picture tube. The picture tube utilised for the above mentioned function in this chassis is specially constructed to limit X-radiation. For continued X-radiation protection, replace tube with the same type as the original HITACHI approved type.

Keep the picture tube away from the body while handling. Do not install, remove, or handle the picture tube in any manner unless shatterproof goggles are worn. People not so equipped should be kept away while picture tubes are handled.

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1 DESCRIPTION

1.1 *A8/D8 MKII MAIN PSU*

From switch on the AC voltage is rectified by the bridge D900 which produces approximately 300V across C918. This is then applied to the collector of Q903 via the primary winding of T900. Initially the voltage on pin 7 of I900 will rise to approximately 16V via R901, D929 and Q905. This allows the internal circuitry of IC900 to generate a sawtooth waveform at pin 4, from which a square wave output is obtained at pin 6. This output is applied to the gate of Q901 which turns on and off, this alters the voltage on the emitter of Q903 causing this device to turn on and off, generating the outputs in the secondary windings of T900.

After initial power up of I900 pin 7 is supplied from the bias winding (pin 18) of T900 via D911 for continued operation. The bias winding voltage is also rectified by D922 which is then supplied to the base of Q905 low via R908/Q906/R924 turning Q905 off, this is done to reduce the power dissipated by R901 once the power supply is running.

A current sense circuit consisting of R910, R939, R922 and R980 feeds back a voltage to pin 3 of I900, MAX voltage approximately 0.8V. Should the applied voltage exceed the reference the pulse width is limited from output pin 6. In this way Q903 is offered protection from changes in primary current.

R909 and C914 act as a soft start circuit, this limits the pulse width output from pin 6 during the initial start up period, allowing a gradual rise to full power. Q909, R918 and associated circuitry are for reducing the frequency of the power supply when the set is in standby. A sense voltage rectified by D922 consisting of R905 and R906, supplied pin 2 of I900, this is then compared to an internal reference voltage. If it exceeds the internal reference the output from pin 6 will be limited by the internal error amp. The secondary voltage induced in T900 winding 7/9 is rectified by D950, producing the HT voltage which is smoothed by C977. In standby the HT rises slightly.

Winding 5/10 produces approximately 10V via D951, which is smoothed by C957. This is then applied to dual DC-DC converters (+8V, +5V out). A control ramp is found on pin 2/6 I900. This ramp is formed by R944/C935, and terminated by Z913, D902, R934 network. Ramp frequency is clamped to the main PSU frequency by the winding on pin 5 T900. This ramp is compared with the feedback level from I902 (+5V) I904 (+8V). The reference device monitors the output and changes the DC level to pin 5. The ramp crosses the DC feedback level, and the output at pins 1/7 goes low. The output at pins 1/7 starts high at the beginning of the ramp, goes low at ramp cross level. This action via Q912, Q911 controls the pulse width and so the regulation of the +8V/ +5V rails. The output pulse width changes with load to maintain the correct regulating voltage.

The output of I910 pins 1,7 are buffered to improve switching losses using a push - pull transistor network Q918, Q917 (for +5V). This transistor network gives fast edge switching of Q912 (+5V) and Q911 (+8V). Over current protection is provided with the current sense resistor RP03. Network Q956 RP04/C966 pull pin 10 of I903 high if high load current is flowing through RP03.

Winding 2/11 produces approximately 16V via D952, which is smoothed by C955 and then applied to Q921 through R974, which is used as a current sense. The output from Q921 supplies 16V for the audio amplifier I401.

HT regulation is controlled by Q954 stage. The base of Q954 is set at a pre-determined level by the resistor network R950, R982 and R953. The emitter of Q954 is held at approximately 6.2V by Z950. Should the HT rise, the base voltage becomes more positive than the emitter, and this difference is amplified by the transistor and applied to optocoupler I901. The output from I901 is then applied to pin 1 of I900 which regulates the HT by altering the duty cycle of the waveform output from pin 6 of I900.

1.1.1 STANDBY SWITCHING

The low voltage supplies are switched off in standby, this is controlled by the micro processor which outputs a high in standby and a low when the set is out of standby. This is then applied to resistors R923 and R940/R977. This ‘high’ is also applied to the base of Q915, Q916, Q910 which in turn terminate operation of the +8V, +5V DC-DC converters, and pull the gate of Q921 low so switching the +16V audio supply to low state. In standby the +B voltage rises slightly to maintain bias winding voltage to pin 7 of I900. To switch the set out of standby the on/off line is switched high by the micro, and Q916, Q915, Q910 are deactivated, causing the +8V, +5V, +16V rails to return to normal operation.

1.1.2 POWER GOOD AND PROTECTION

I903 is made up of 4 comparators, the power good line uses comparator 2. Pin 5 is used as the reference which is held at 2.5V by I905 supplied by pull up resistor R968. Pin 4 uses R961/R962 and R955/R959 as a potential divider which is connected between the +10V and T900 winding through D959 which is in forward converter mode. In operation this means pin 4 is held below the reference level of pin 5 until the mains supply is interrupted or the set is switched off at which time pin 4 rises above pin 5 and the output pin 2 is pulled low. This low is sensed by the micro. In normal operation pin 2 is held high by pull up resistor R990 from the 5V supply.

The protection line (pin 14) is held high under normal running conditions by R971 from the 5V supply, this high is applied to the protection line to the micro. When the protection line is pulled low the set goes into standby mode, the set can be restarted by the usual methods of bringing the set out of standby, but until the cause of the protection circuit operation is removed the set will return to its standby state.

The over current for the 16V audio supply uses comparator 1, a reference voltage is set up on pin 6 by resistors R967, and R964. The voltage being compared is fed to pin 7 using the potential divider R968 and R966 which is supplied from the output side of the current sense resistor R974. Should the voltage on pin 7 fall below that of pin 6, pin 1 will be pulled low, thus pulling the protection line low via D958 putting the set into standby.

Comparator 3 is used to protect against a layer short within the FBT, it will also act as protection for a short on the secondary outputs of the FBT. I903 is supplied with approximately 16V via D960 to pin 3, from this supply a reference voltage is fed to pin 9 using potential divider R972/R969, fed via Z948 supply. Pin 8 is supplied by another potential divider this time made up of three resistors R973/R970 and R760 samples the current flowing through Q752, should this increase, the voltage drop across R760 will increase and raise the voltage of pin 8, when it exceeds pin 9, pin 14 will be pulled low, putting the set into standby.

Comparator 4 is used for EHT/over voltage protection, as all the FBT secondary voltages are proportional, the 200V supply to the CRT base is used to generate the voltage to be used in comparison, this is done by using a potential divider made up of R718, R749 and R719. Z708 monitors the voltage at the junction of R718 and R749, if this exceeds 36V, the Zener diode conducts, applying a high on pin 10 of I903, this is compared with the reference voltage on pin 11, which also uses the 2.5V set up by I905. When pin 10 is higher than 2.5V, pin 13 is pulled low, in turn pulling the protection line low via D957, putting the set into standby.

The LT lines are given protection using diodes D931, D932 and D930, these are connected in reverse bias from the prot sense line to the 8V and 5V. The +5V standby link is protected by D986, pulling the reference Z950 low if a short is seen on the output of I952. The +16V phono out has a diode back to I903 pin 5 in case of short.

If the +B or audio supply lines become short circuit to ground before the protection on the secondary of the power supply, the primary over current protection (I900 pin 3) will operate, turning off the drive output from I900 pin 6. A latch circuit Q955/R998/RP01/C964, will operate to turn the power supply into standby (under fault condition) if the software fails to act on I903 pin 14 low. Delay before latch set by C964/R994. The +B is given protection from overvoltage via Z907, Z907 goes short circuit if the +B voltage rises above 180V DC.

1.2 DTI PSU

1.2.1 CIRCUIT DESCRIPTION

The mains is switched on via the {TV on}. At this point the AC mains is rectified by D9019, D9001, D9002, D9003 which produces approximately 340v DC across C9026. This is then applied to the collector of Q9000 via the primary winding of T9000. Initially the voltage on pin 7 of I9000 will rise to approximately 16v via R9001, D9000, this allows the internal circuitry of I9000 to generate a sawtooth waveform at pin 4 from which a square wave output is obtained at pin 6. This output is applied to the gate of Q9005 turning the MOSFET on and off, pulling the base/emitter high and low accordingly reducing cross over, generating the outputs in the secondary windings of T9000.

After initial power up pin 7 of I9000 is supplied from the bias winding pin 3 of T9000 via D9010 for continued operation hence R9001 unable to provide running current demand for I9000 [200mA approx].

A current sense circuit consisting of R9057, R9013 and R9015 feeds back a voltage to pin 3 of I9000, this voltage is compared with an internal reference voltage of approximately 0.8V, should the applied exceed the reference, the pulse width is limited from output pin 6 [chip in over current mode]. In this way Q9005 is offered protection from changes in primary current. Secondary overvoltage protection is offered also by R9009, should the feedback be disabled then the secondary voltage will be limited to safe levels, the output from pin 6 will be limited by the internal error amplifier and internal reference.

R9006 and C9010 act as a soft start circuit, this limits the pulse width output from pin 6 during the initial start up period, allowing a gradual rise to full power. ZD9000 and ZD9001, ZD9006 will go short if Q9000 should go short, protecting I9000 and Q9005.

The secondary voltage induced in T9000 winding 10/14 is rectified by D9031 producing 30V which is smoothed by C9041.

Winding 12/14 produces 5V at 1.5A then rectified by D9026 and smoothed by C9037 and C9036. This voltage rail, being the highest current rail is used for regulation via I9002, providing feedback to pin 1 of I9000. From the 5V rail, a 3V3 rail is extracted at 2.7A. The current output is controlled by a PWM circuit consisting of switching MOSFET Q9003, gate drive is provided by Q9002 and Q9004 and pin 1 of I9004, pin 2 of I9004 is supplied by a sawtooth waveform shaping circuit consisting of D9022, Z9003, R9036, C9032. Pin 3 is supplied by varying DC levels via I9003. The 3V3 voltage rail is regulated by I9003.

Winding 13/15 provides 16V from D9018 and smoothing caps C9046 and C9024, also a 9V rail is provided by I9005 regulator. –16V rail is provided by D9017 and smoothing caps C9022 and C9045.

SECONDARY PROTECTION: Provided via I9004 pin 7. Pin 6 of I9004 is set to a steady voltage level around 3V, pin 5 is used as the over current sense point, D9023, D9034, D9029 is used to pull down pin 5 below pin 6 during over current, in this state pin 7 is low which in turn disables the feedback point pin 1 of IC9000 shutting down the power supply.

1.2.2 FEEDBACK OPERATION

Increase in load demand by secondary rails results in higher voltage feedback on the cathode of I9002 in turn rising the voltage on pin 1 of I9000 this voltage is compared to the sawtooth generated on pin 4 via R9011 and C9013, this produces the gate drive square pulse with larger off time, therefore the larger the load demand the larger the duty cycle and vice versa.

1.3 SCAN VELOCITY MODULATION

During transmission the signal suffers from degradation and also due to the frequency characteristics of the television circuitry. This normally results in a gentle rise or fall in the luminance change areas when black-to-white-to-black patterns are received.

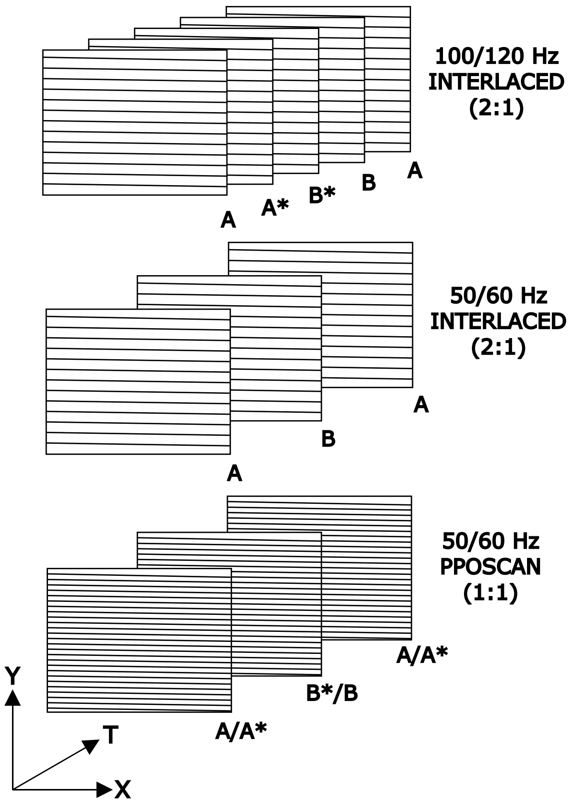
The picture sharpness quality can be assessed by how steep the leading and trailing edges are. The scan velocity modulation circuit has been designed to improve picture quality, i.e. make the video signal edges steeper, by controlling the horizontal scanning velocity of the electron beam in the CRT.

The velocity modulation circuit produces a compensation signal by adding the RGB components then differentiating. The compensation signal is given some current gain, applied to the auxiliary coil (connector E806) on the neck of the cathode ray tube (CRT).

The VM circuit is located on the CRT base along with the final RGB amplifiers. The RGB signals derive from PL803 pins 2-4 and into emitter of Q861, through the differentiator C865, R892 and R893 arriving at the base of Q862 for voltage amplification and latter stages power gain. Final VM pulses arrive at E806 to VM coil around tube neck.

1.4 DIGITAL DOUBLE-SCAN CONVERSION UNIT (FEATURE BOX)

The main feature of this unit is double scan frequency conversion, 100/120Hz interlaced and 50/60Hz progressive scan. Other features of this unit are CTI (Colour Transient Improvement), horizontal compression, noise reduction, sharpness and vertical zoom & freeze. These functions are controlled by I^{2}C bus and are provided elsewhere by the picture improvement IC, TDA9178 (IE01) for 50Hz models without a Feature Box.



As the diagram shows, A/B are the Odd/Even original 50Hz signal fields which are used to create extra picture information, while A*/B* are the predicted/manipulated extra picture information, created by the feature box. The diagram shows the differences between 100/120Hz interlaced and 50/60Hz progressive scan. The biggest advantage of progressive scan is "non-interlaced" scanning; keeping the field frequency at 50/60Hz. This means the line construction is double per field, compared with 100/120Hz interlaced. It will make very fine pitch scan lines and will eliminate line flicker. The advantage of selecting 100Hz operation will be the reduction of large area flicker and reduce line flicker (except 523 50Hz models).

This unit is powered from +5V and +8V supplies, feeding into pins 21, 22 and 26 of E10 respectively. The three input 50Hz video signals Y, U, V are sent to this unit at pins 8, 10 and 12 of E11. The Y, U, V video output signals (double frequency video) are taken from pins 5, 3 and 1 of E11. Horizontal and vertical input sync signals are taken from composite signal at pin 24 of E10, the double frequency horizontal and vertical sync signals outputs are from pins 30 and 31 of E10.

1.5 INPUT PROCESSOR (TDA 9320)

The TDA 9320 (I200) is a multi-standard input processor.

Features include:

1.5.1 VIDEO OUTPUTS/EXTERNAL INPUTS

The input processor has provision for three CVBS inputs (1 internal & 2 external) and 2 Y/C inputs. The external CVBS inputs are used for the SCART sockets. The Y/C inputs are used for S-VHS and a third CVBS input. The circuit can detect whether CVBS or a Y/C signal is presented to AV3, or AV1 inputs. The IC has 2 RGB inputs with fast switching. The switching of the various sources is controlled by I^2C and detection of a Comb filter can be made.

Only one RGB input is used for connection of eternal RGB equipment. These are pins 36, 37, 38 (RGB) & pin 39 (blanking).

1.5.2 SYNCHRONISATION

The sync separator is preceded by a controlled amplifier which adjusts the sync pulse amplitude to a fixed level. These pulses are fed to the slicing stage which is operating at 50% of the amplitude. The sync pulses are fed to the phase detector and to the coincidence detector. This coincidence detector is used to detect whether the line oscillator is synchronized and can also be used for transmitter identification. The PLL has a very high statical steepness so that the phase of the picture is independent of the line frequency.

For the horizontal output pulse, two conditions are possible:

1. An HA pulse which has a phase and width which is identical to the incoming horizontal sync pulse.

2. A clamp pulse CLP which has a phase and width which is identical to the clamp pulse in the sandcastle pulse.

The HA/CLP signal is generated by means of an oscillator which is running at a frequency of 440 x FH. Its frequency is divided by 440 to lock the first loop to the incoming signal. The free running frequency of the oscillator is determined by a digital control circuit which is locked to the reference signal of the colour decoder. When the coincidence detector indicates an out of lock situation the calibration procedure is repeated.

The vertical pulse is obtained via a vertical count down circuit. The countdown circuit has various windows depending on the incoming signal (50/60Hz).

1.5.3 VISION IF AMPLIFIER

The video signal is demodulated by means of a PLL carrier regenerator. This circuit contains a frequency detector and a phase detector. During acquisition the frequency detector will tune the VCO to the right frequency. After lock-in, the phase detector controls the VCO so that a stable phase relation between VCO and the input signal is achieved. The VCO is running at double the IF frequency with the reference signal for the demodulator obtained by means of a frequency divider circuit.

The AFC output is obtained by using the VCO control voltage of the PLL and can be read via the I^2C bus. The AGC detector operates on top sync and top white level. The time constant on the AGC system during positive modulation is long to avoid visible variations of the signal amplitude. To improve the speed of the AGC system a circuit has been included which detects whether the AGC detector is activated every frame period. When during 3 field periods no action is detected the speed of the system is increased. For signals without peak white information the system switches automatically to a gated black level AGC. Because a black level clamp pulse is required for this way of operation the circuit will only switch to black level AGC in the internal mode.

The circuit contains a video identification circuit which is independent of the synchronisation circuit. Therefore search tuning is possible when the display section of the receiver is used as a monitor.

1.5.4 CHROMA & LUMA PROCESSING

The IC contains a chrominance bandpass filter, the SECAM cloche and chrominance traps. The filters are calibrated using the tuning frequency and the crystal frequency of the colour decoder. The luminance output signal which is derived from the incoming CVBS or Y/C signal can be varied in amplitude by means of a separate gain control.

1.5.5 COLOUR DECODING

The colour decoder can decode PAL, NTSC and SECAM signals. The PAL/NTSC decoder contains an alignment free crystal oscillator with 4 separate pins, a killer circuit and two colour difference demodulators. The 90o phase shift for the reference signal is made internally. Because it is possible to connect 4 different crystals to the colour decoder, all colour standards can be decoded without external switching circuits. Crystals not used must be left open. The horizontal oscillator is calibrated by means of the crystal frequency of the PLL.

The IC contains an automatic colour limiting circuit which is switchable which prevents over saturation when signals with a high chroma-to-burst ratio are received. The ACL circuit is designed such that it only reduces the chroma signal and not the burst. This has the advantage that the colour sensitivity is not affected by this function.

The SECAM decoder contains an auto-calibrating PLL demodulator which has two references, the 4.43MHz sub-carrier frequency which is obtained from the crystal oscillator which is used to tune the PLL to the desired free running frequency and the bandgap reference to obtain the correct absolute value of the output signal. The VCO of the PLL is calibrated during each vertical blanking period, when the IC is in search or SECAM mode. The base-band delay line is integrated into the package.

CVBS outputs for Teletext, Comb Filter and monitor outputs are available.

1.6 PICTURE IMPROVEMENT (TDA9178)

The picture improvement IC is an analogue video processor offering three main processing functions; luminance vector, colour vector and spectral processing. Features presently being implemented are; luminance transient improvement (LTI), colour transient improvement (CTI), variable gamma control and picture dependant non-linear Y and U, V processing by luminance histogram analysis.

The spectral processor provides luminance transient improvement, luminance detail enhancement by smart peaking and colour step improvement (CTI). The line width control may be user defined. The luminance vector processor, the transfer function is controlled in a non-linear manner by histogram analysis of measured luminance values measured in a picture. As a result the contrast ratio of the most important parts of the scene will be improved. A variable gamma function after the conversion offers the possibility of alternative brightness control or factory adjustment of the picture tube.

The following functions sharpness, noise reduction and colour transient improvement (CTI) are provided by the picture improvement IC for 50Hz models, while 100Hz/progressive scan models provide these functions within the double scan module (feature box). All functions described are switchable/adjustable via I^2C control using the options in the service menu.

Y, U and V signals are taken from I200 pins 49, 50 and 51 and go straight into Yin U_{in} and V_{in} (pins 6, 8 and 9 of IE01). The enhanced Y, U and V outputs originate from IE01 (pins 19, 17 and 16 respectively) and are directed to IZ04 (pins 28, 27 and 26 respectively).

1.7 TUNER

The tuner U100, is a frequency synthesis type with an unbalanced input and IF of 38.9MHz, powered from the +5V rail while the tuning voltage is supplied by the +33V rail, supplied from the horizontal deflection circuit. Direct frequency access, channel selection, AGC and AFC functions are controlled via the I^2C bus. AGC, AFC and Offset controls may be selected by entering the service menu and selecting the ‘tuner’ option.

Pin 1, AGC is taken from pin 62 of TDA9320/9321 (I200). The balanced IF output is taken from pins 10 and 11 arriving at both inputs of the vision and sound SAW filters (pins 1 and 2). The outputs from X200 and X202 (pins 4 and 5 respectively) pass through to pins 2 and 3 and pins 63 and 64 of I200, where they are demodulated.

1.8 RGB PROCESSOR (TDA9330)

1.8.1 VERTICAL DEFLECTION AND GEOMETRY CONTROLS

The drive circuit for the vertical and E-W deflection circuits are generated by means of a vertical divider which gets its clock from the line oscillator. The divider is synchronised by the incoming vertical pulse generated by the input processor (50Hz models) or the feature box.

The vertical drive is realised by means of a differential output current. The outputs (100Hz/progressive scan models) must be DC coupled to the vertical output stage. The vertical geometry can be adjusted by I^2C control via the service menu.

1.8.2 HORIZONTAL SYNCHRONISATION AND DRIVE CIRCUIT

The horizontal drive signal is obtained from an internal VCO which is running at a frequency of 13.75MHz. This oscillator is stabilised to this frequency by means of a resonant oscillator 12MHz. The internal VCO is synchronised to the incoming horizontal HD pulse by means of a PLL with an internal time constant. The horizontal drive signal generated by means of a second control loop which compares the phase of the reference signal from the internal VCO with the flyback pulse. The time constant loop is internal. The IC has a dynamic horizontal phase correction input which can be used to compensate phase shifts which are caused by beam current variations. Additional settings of the horizontal deflection which are realised via the second loop are the horizontal shift and the parallelogram correction.

The horizontal drive signal is switched on and off via the so called soft-start/soft-stop procedure. This function is realised by means of a variation to the Ton of the horizontal drive pulse. For EHT generators without bleeder the IC can be set in a fixed beam current mode. In that case the picture tube capacitance is discharged with a current of about 1mA which is determined by the black current feedback loop. With the fixed beam current option activated it is still possible to have a black screen during switch-off. This can be realised by placing the vertical deflection in an overscan position.

An additional function of the IC is the low-power start-up feature. This mode is activated when a supply voltage of 5V is supplied to the start-up pin. The required current for this function is 3mA typical. In this condition the horizontal drive signal has the normal T_{off} and T_{on} grows gradually from zero to about 30% of the normal value. This results in a line frequency of about 50KHz or 25KHz. The output signal remains unchanged until the mains voltage is switched-on. Then the horizontal drive signal will gradually change to the normal frequency and duty cycle via the soft-start procedure.

The IC has a general purpose bus controlled DAC output with a resolution of 6 bits and with an output voltage range between 0.2V to 4V.

1.8.3 INPUT SIGNALS

The RGB control circuit of the TDA9330 (IZ04) contains three sets of input signals.

Y, U, V, input signals which are supplied by the input processor or feature box. The nominal input signals for u and V are 1.33 $V_{Peak-to-Peak}$ and 1.05$V_{Peak-to-Peak}$ respectively. These input signals are controlled by brightness, contrast and saturation.

Two RGB sources are intended for use by the SCART, while the second is used for the OSD and Teletext. The required input signal has an amplitude of 0.7$V_{Peak-to-Peak}$. The switching between the internal signal and the OSD signal can be realised via a fast blanking . this input is only controlled by brightness.

Switching between various sources can be realised via the I^2C bus and by fast insertion switches. The circuit contains switchable matrix circuits for the colour difference signal so that the colour reproduction can be adapted for PAL/SECAM and NTSC.

1.8.4 OUTPUT AMPLIFIER

The output signal has an amplitude of around 2V black-to-white at nominal settings. The required white point setting of the picture tube is implemented by 3 separate gain settings for the RGB channels.

To obtain an accurate biasing of the tube, a continuous cathode calibration circuit is implemented by means of a two point black level stabilisation circuit. By inserting 2 test levels for each gun and comparing the resulting cathode currents with two different reference currents, the influence of the picture tube parameters like the spread in cut-off voltage can be eliminated.

1.9 SIGNAL PATH DESCRIPTION

The IF signal is obtained from SAW filters X200 (vision) and X202 (Sound) pins 4 and 5 and are fed into pins 2 and 3 vision and 63 and 64 sound of I200. A composite video signal is available at pin 10 from the vision demodulator. IF sound out from pin 6. The video is taken from pin 10 via C304 into pin 12 and out at pin 13. This is the selectable Group Delay via software input output. The composite video gets taken through buffer and filtering stages where the desired video returns to I200 at pin 14.

The AV switching matrix supports two SCART sockets, phono CVBS and S-VHS inputs. SCART CVBS inputs are at pins 20 (AV1 E301) and 16 (AV2 E302), CVBS outputs to SCART pins 19 from emitter of Q301 (AV1) and emitter of Q303 (AV2). The RGB input (Digital models) to I200 from the Digital Terrestrial Tuner (DTT) comes to pins 36-38, from P301 pins 9, 7 and 5, respectively. S-VHS input is via E300 to pin 23 and 24 of I200, detection of CVBS input is detected within I200. For models with progressive scan feature, detection for a Comb filter has been fitted via Y/C input pins 28 and 29. Colour sub-carrier output for the Comb filter is from pin 30.

Y, U and V signals are taken from I200 pins 49, 50 and 51 and go straight into Yin Uin and Vin (pins 6, 8 and 9 of IE01) for 50Hz operation, while 100Hz operation, Y, U, V signals are directed to pins 9, 10 and 12 of the double scan module (UQ01).

Other miscellaneous pins such as the sandcastle pin 59 is independent of the sandcastle pulse generated by I200, they do not drive each other. The Vertical and Horizontal output pulses generated by I200 drive the double scan module, pins 18 and 19 respectively (100Hz operation) or the IE02 (50Hz operation) pins 23 and 24. I^{2}C control lines are pins 46 and 47, and tuner AGC control voltage is present at pin 62.

As already previously described Y, U, V signals in either 50Hz/100Hz/Progressive scan mode are sent to pins 26-28 of the TDA 9330/31 (IZ04). Once inside the RGB processor, geometry and synchronisation functions can be implemented before being sent to the CRT base (pins 40-42 of IZ04 and 3-5 of PZ02) for final video amplification and to the velocity modulation circuit.

The vertical drive output is provided by pin 1 and 2 of IZ04 directly to I601 Vertical Output IC (pins 11 and 12). Horizontal output is from pin 8 of IZ04 and feeds the base of Q701 Bipolar (50Hz), Q701B MOSFET (100Hz). East-West drive output can be obtained at pin 3 and is driving the gate of the East-West MOSFET Q700.

I^{2}C is present at pins 10 and 11 (IZ04) and +8V supply rails at pins 7 and 17. Two sets of RGB inputs are available, only one set is used for the OSD, pins 35-37, the other is for a VGA board which is not fitted.

A CVBS monitor output is taken from pin 28 of I200 and is sent to pin 61 of I001 (Microprocessor) where the text is decoded. CVBS monitor output is also sent to SCART 1 pin 19 to monitor what is being displayed. Pin 19 of SCART 2 outputs signal from RF.

1.10 AUDIO CIRCUIT

The output from the Tuner T1 is fed via a gain and buffer stage formed by Q200 and Q201 to the Saw Filter X202. The saw filter has two separate characteristics depending on which of the two inputs (on pin 1 and 2 of the Saw Filter) the signal is applied to. Selection is achieved by the combination of Q204 and Q203. For most standards, pin 1 is selected. However, when an L' Signal has been selected, the micro (I001) instructs I200 via an I^{2}C command to take pin 19 high. When this happens Q204 conducts taking pin 1 low and switching Q203 and D203 off. This means that the collector of Q203 goes high allowing D202 to conduct and hence the signal to be applied to pin 2. To return to other broadcast standards, pin 19 of I200 is obviously returned to the low condition.

The output of the Saw is applied to pins 63 and 64 of I200. Here the signal is transformed from the 1st IF (30 – 40MHz depending on transmission standard) to the sound IF (5.5MHz to 6.5MHz depending on the transmission standard).

I200 also provides AM demodulation for the L' and L standards. The demodulated signal appears superimposed on the Sound IF on pin 5 of I200.

This signal then takes two paths, the first takes it through a Low pass filter formed by R426 and C427 and coupling capacitor C426. This is then applied to pin 55 of I400 and forms the AM Sound Input. The second path takes the signal through an amplifier and buffer stage formed by Q400 and Q401.

After these stages some high pass filtering is applied by C464 and R477 before the sound IF is applied to pin 60 of I400 via C431.

I400 is The MSP3410D. This IC provides NICAM, FM Mono and FM Stereo Demodulation as well as matrixing of the SCART/digital receiver signals (If fitted).

The AV1 input is applied on pins 52 and 53, the AV2 input on pins 49 and 50, the AV3 input on pins 46 and 47. The Digital input (DTT) is applied to pins 43 and 44 (when fitted). In each case a 100R resistor and 330nF capacitor is used.

The SCART outputs on I400 use the following protocol.

SCART Output	Output Signal	
	Non Digital Models	**Digital Models**
AV1	RF	Digital
AV2	Selectable or Auto*	Selectable or Auto*

*If auto is selected in the on screen menus, AV2 follows the audio of what is being watched.

The device is I^{2}C controlled via pins 10 and 11 and receives a reset from the micro at power-up on pin 24. The clock is provided by X406 on pins 62 and 63. The device has three supply rails, 5V Digital (Pin 18), 5v Analogue (Pin 57) and 8v Analogue (Pin 39).

1.11 DOLBY DECODER (Prologic Models)

The Dolby decoding is provided by IF01 (YSS241).

The signals which are sent to this device from I400 in the I2S format are:

SD0 (Pin 13 Of I400) - the Left and Right channel data (before Dolby decoding)

SCK (Pin 11 Of I400) - the system or bit clock

WS (Pin 12 Of I400) - the word select line, provides selection between the Left and Right samples on the SDO Line.

IFO1 is provided with an 18.432MHz clock via pin 1 of I400 (SYSCLK), a reset line from pin 4 and is I^{2}C controlled. The Pro-logic signals that the device decodes are provided in I2S form at pins 40 and 41 (DACS1 and DALR). These signals are in a 32bit per channel format (The MSP4310D uses 16 bit) and must therefore pass through a conversion IC IF02. This IC also takes a Bit clock DABC from pin 36 of IF01. IF02 then provides the 16 bit pro-logic I2S channels as SDI1 and SDI2 on pins 14 and 20 of I400.

I400 then passes these signals through DAC's so that the Left, Right, Centre and Surround signals appear at pins 29, 28, 26 and 25 as Pre-L, Pre-R, Pre-C and Pre-S respectively. These are then amplified by 3dB by op-amp IF03 to become AmpL, AmpR, Centre and Surround. These then pass through a buffer and filter network to the four way phono plug JF01. The AmpL and AmpR signals split off before the buffers to the amplifier I401 via dividing resistors R443/R439 and R446/R447 and are decoupled by C443 and C445. The operation of the amplifier is explained elsewhere in this manual.

1.12 DIGITAL AUDIO

1.12.1 SUPPLY RAILS

The Digital Audio decoder board consists of a 4 layer PCB and is situated above the Audio amp board. The 8v supply for the Digital Audio decoder arrives at pin 4 of PS06. It is then passed to the 5v regulator IS16 via LS02. It then reappears at the output of the regulator as 5VM. This rail is split into 5VA and 5VD via inductors LS05 and LS06 and is decoupled by CS63, CS64, CS65 and CS66 respectively. The two rails then supply the DAC's IS06, IS07 and IS08, the SPDIF Receiver IS05, the clock generator IS15 and the DAC output buffers QS05, QS06, QS07, QS08, QS09 and QS10. 5VD is also made available for the optical receiver on the amplifier board via the connector PS07.

5VM goes to the 3V3 regulator IS13. This rail then supplies the main decoding IC IS01, the SRAM IS02, IS03 and IS04, the EEPROM IS12, the I^{2}C level translator IS09 and the signal multiplex IS10. Finally, there is an option for a 1V8/2V5 rail via regulator IS14, which can be fed either by the 3V3 or 5VM rail. This will supply certain pins of The DSP processor IS01 should the device change over to this style.

1.12.2 I^{2}C CONVERSION, DSP MAIN CLOCK AND RESET

The DSP56362 (IS01) is controlled by the I^{2}C lines (SDA and SCL) from the micro, which come from the header E304 on the main board. The signal travels via a nine way lead arriving at pins 8 and 9 of PS04 on the decoder board.

Since the DSP56362 is a 3V3 device and the Micro is 5V, some level translation of the I^{2}C is required. This is achieved by IS09. This device also acts as a buffer for the Main Clock for the DSP, which also travels on the 9 way lead described above before arriving at pin 5 of PS04. It then goes to pin 5 of IS09 as MSP12SCLK and leaves pin 6 as DSP Extal. This 1.024MHz signal is then up-converted within the DSP to the various clocks required. IS01 is reset on pin 44 via a line from the 9 way lead at pin 7 of PS04.

1.12.3 MUTING

The DACs IS06, IS07 and IS08 are muted via pin 34 of IS01 going low. Additional mute lines are provided for the Amplifier board on pins 41, 42 and 43 via the three way header PS08. In either case, the mute lines are activated via I^2C commands.

1.12.4 MODES OF OPERATION

Although described as the Digital Audio Decoder board, this board in fact provides audio in both the Analogue and Digital Audio modes. The following is a description of this board operation in the two different modes.

ANALOGUE MODE

This mode is used when either a SCART, Phono or RF signal provides the Audio source.

In analogue mode, the analogue signal, be it RF or from a SCART/Phono source, is first processed by I400, the MSP3410D on the main board.

This device converts the signal to 16 bit I2S format consisting of a Word Select (pin 12), Data (pin 13) and Bit Clock line (pin11). The signals arrive at PS04 on the decoder board via the 9 way lead described above.

The 18.432MHz clock signal from pin 1 of the MSP3410D is connected to a two way header E28. From here it is passed via a shielded lead to PS01 on the decoder board. The signal is then passed through a buffer amplifier stage formed by QS11 and QS12 before being transformed to a 8.192MHz Clock by IS15.

On the Decoder Board, Analogue mode is selected by instructing IS01 via an I^2C command to take pin 28 of IS01 (the SPDIF select line) high. This signal is then inverted by QS01 thus pulling pin 1 of IS10 low. This Multiplexer then switches the Word Select, Data, Bit Clock and 8.192MHz clock mentioned earlier to the DSP56362 (IS01). The 8.192MHz clock is also passed to the DACs IS06, IS07 and IS08.

The output of QS01 is also fed to pin 23 of the DACs, thus switching the devices to 16 bit. (leaving the device in 24 bit results in distorted sound).

The DSP carries out either Stereo or Pro Logic decoding of the signal, setting the volume and Graphic Equaliser to the level selected by the user and also the channel outputs to their desired settings (i.e. if no centre has been selected in the speaker setup menu and the device is in the Pro Logic mode, it redirects the centre to the Left and Right channels).

The DAC signals then emerge (depending on mode) for the Front Left and Right, Rear Left and Right, and Centre and Subwoofer on pins 4, 5 and 6 respectively of the DSP56362. They are then converted by the DACs to Analogue form after which they are buffered by QS05, QS06, QS07, QS08, QS09 and QS10 before being passed to the Audio Amplifier board via header PS03. Here, 6dB is added to the main channels and 9.5dB to the Subwoofer channel by Op Amps I408, I409 and I410 before being passed to the output buffers (phono outputs) and power amplifiers (speaker outputs). This operation is described more thoroughly in the description of the Audio amplifier board itself.

DIGITAL MODE

This mode is used when either a coaxial or optical digital audio signal is the selected source

The operation in Digital Mode is similar to the Analogue mode except in this case the signals are not derived from the MSP3410D but instead come from the SPDIF receiver CS8414 (IS05). This device takes signals on pins 9 and 10 from either the coaxial socket or optical receiver on the amplifier board via a 4 way shielded lead connected to PS07. If both sources are connected, the optical receiver takes priority.

IS01 (the DSP56362) provides the device with 6.144MHz clock on pin 13 in order that status and error information can be returned on pins 2, 3, 25 and 27. IS01 also provides a reset for the SPDIF by taking pins 17, 18, 23 and 24 high via pin 32 of IS01 applied at switch on, this reset is sometimes re-applied by the DSP if invalid data is received.

The SPDIF Receiver converts the PCM or Digital Audio bit-stream to I2S format which appears as SPDIFWS, SPDIFSCK, SPDIFMSTRCLK and SPDIFI2SDATA, on pins 11, 12, 19 and 26 of the device respectively. This is passed to the DSP and DACs via the multiplexer, which is switched via pin 28 of IS01 going low and thus the output of QS01 going high. This also switches the DACs to 24 bit mode.

Three of the I2S signals (SPDIFWS, SPDIFSCK and SPDIFI2SDATA) are passed to the DSP where they are processed according to the user settings and there format into either a Dolby Digital, DTS, MPEG Multi-channel, PCM Prologic or PCM Stereo signals before being passed out to the DACs (which have the SPDIFMSTRCLK provided to them via the multiplexing IC). The Audio signals then pass to the amplifier board in the same manner described above.

In DTS Mode extensive use is made of the EEPROM IS12 as this holds the decoder coefficients.

The SRAM, IS02, IS03 and IS04 is made use of extensively in both Dolby Digital, DTS and MPEG Multi-channel modes. The SRAM integrity can be confirmed by looking for a code in the fault diagnostics software. A fault here will normally manifest itself as a distortion in the Surround channels.

NOTE: Due to the nature of Digital Audio and in particular Dolby Digital, DTS and MPEG Multi-channel, it may sometimes appear that channels aren't working when either the user has disabled them in the speaker setup menu or the software they are using doesn't support that channel (i.e. no centre from a Dolby Digital 2/2.1 source)

For this reason, before carrying out tests for missing audio on individual channels, please use a DVD player to check that:

The Sound mode is Dolby Digital, DTS or MPEG Multi-channel (or Pro Logic if your disc isn't playing yet)

The speakers are set to either small or large (and not none!) in the speaker setup menu

The power amplifiers are set to ON in the speaker setup menu.

The disc you are playing is encoded in the 3/2.1 format, (This can be confirmed by pressing the info/recall button on the handset when the disc is playing)

You can then check for the signals at the DAC outputs with an oscilloscope.

1.13 AUDIO AMPLIFIER

1.13.1 AUDIO AMPLIFIERS MAIN BOARD

The amplifier for the left and right channels on the main board is a ST Microelectronics TDA7297, a dual bridge 2x 15W IC. It requires an 18V supply to achieve 15W into 8W speakers.

Table below shows IC pin connections:

Pin	**Function**	**Pin**	**Function**
1	Left output positive	9	Signal ground
2	Left output negative	10	Not connected
3	+18V supply	11	Not connected
4	Left signal input	12	Right input
5	Not connected	13	+18V supply
6	Mute control	14	Right output negative
7	St-by control	15	Right output positive
8	Power ground		

At turn ON and OFF, I001 turns Q403 on, holding pins 6 and 7 low keeping the amplifier turned off stopping pops through the speakers.

When the front amplifier is turned off using the software option in the installation/speaker set up menu the amplifier is turned off by I001 controlling Q402 which holds pins 6 and 7 low.

The left and right signals are supplied from the Audio Amplifier panel via P303 pins 2 and 3.

The left signal is input through the potential divider network of R443/R439, capacitor C442 into pin 4 of I401. The right signal is input through the potential divider network of R446/R447 capacitor C444 into pin 12 of I401.

On Dolby models a DIN board containing 2 switched speaker sockets is connected into the speaker leads connected to P400. On non-Dolby models the speaker leads connect directly into P400.

For the 32" the outputs from pins 1 and 15 of I401 are input to pins 6 and 4 of J400 the headphone socket respectively these are then output from pins 7

E17	Connection	E18	Connection
1	Headphone right signal output.	1	+18V return from headphone switch
2	Right speaker output return from front panel.	2	Left speaker output to front panel.
3	Right speaker output to front panel.	3	Left speaker output return from front panel.
4	+18V supply to headphone socket switch.	4	Ground.
5	Headphone left signal output.		

and 5 and applied to pins 1 and 4 of P400.

The return paths from pins 2 and 3 of P400 go directly to pins 2 and 15 of I401.

For the 36" the headphone socket is on the front control panel and is connected via E17 and E18.

Headphone Circuit

When a 3.5mm jack plug is inserted into the headphone socket the connections between pins 6 and 7 (left channel), pins 4 and 5 (right channel) and pins 8 and 9 (headphone inserted indicator) are broken. The signals for the headphone outputs are taken from one half of each of the left and right power amplifiers (pins 1 and 15 of I401) via C438/R438 and C437/R437 which are input to pins 2 and 3 of J400 respectively. The headphone return is through pin 1 of J400 to ground, this method is used to restrict the maximum power available at the headphones.

The 18V output from pin 8 of J400 is used in 2 ways. The first is to supply the single phono output at the rear of the chassis to power the IR surround speaker transmitter. The second the 18V is sampled by the potential divider made up of R474 and R473 with the midpoint being fed to the microprocessor pin 19 via R045, when this pin is low the software goes into "headphone mode".

WARNING - Neither output for either channel is connected to the chassis ground so caution must be taken if an oscilloscope and other mains operated equipment with a common earth is used simultaneously when checking the amplifier outputs.

1.13.2 AUDIO AMPLIFIER PANEL (CTV)

The Audio Amplifier panel has four distinct functions:

Optical and phono inputs for the digital decoder.

Amplification of the analogue signals.

Phono outputs for the analogue signals to be amplified externally of the set.

Power amplification of the centre, sub woofer, rear left and right channels.

The single phono socket E408 marked coaxial is for inputting digital signals (electrical) and the socket directly above it, I407 marked optical is for inputting digital signals (using laser light and optical link). I407 converts the optical signal into electrical pulses.

These are outputted from the Amplifier board to the Digital Decoder panel via E419.

The Analogue signals output from the Digital Decoder are input to the Amplifier panel at E414, these are applied to operational amplifiers I408, I409 and I410. These Op Amps are powered from the +17V supply used by the Audio Power Amps. Because of the gain required these devices are quad Op Amps with half of each IC (two Op Amp stages) being used for each channel.

	First Stage Input	First Stage Output	Second Stage Input	Second Stage Output
Front Left	I410 Pin 5	I410 Pin 7	I410 Pin 10	I410 Pin 8
Front Right	I409 Pin 3	I409 Pin 1	I409 Pin 12	I409 Pin 14
Centre	I410 Pin 3	I410 Pin 1	I410 Pin 12	I410 Pin 14
Sub-Woofer	I408 Pin 5	I408 Pin 7	I408 Pin 10	I408 Pin 8
Rear Left	I409 Pin 5	I409 Pin 7	I409 Pin 10	I409 Pin 8
Rear Right	I408 Pin 3	I408 Pin 1	I408 Pin 12	I408 Pin 14

The outputs of the Op Amps are then connected to two different paths, one goes to the phono outputs via a single transistor buffer stage, the other to the power amplifiers. The 12V supply for the buffer stage is derived from the +17V via Z415, a 4V7 zener diode.

All the phono output stages are the same so the centre will be used as an example. The signal from I410 pin 14 passes through R493 to the base of Q415, the output from the emitter then passes through R473 and C483. R466 gives the required output impedance, C484, L424 and C485 are a filter network to reduce the EMC emissions. Transistor Q431 is used to mute the phono output and is controlled by the microprocessor via the lines marked MUTE. The signal is then output from the phono socket block E401.

The Audio Amplifiers uses are ST Microelectronics TDA7482 25W mono class D IC’s, they are powered by 2 rails one positive, the other negative, in this application +/- 17V are used.

Audio power output requirement for the CTV is 15W for front left and right (amplifier on the main board), centre, rear left and right. 25W is required for the bass/sub woofer/LFE channel, this is achieved by connecting the output of I401 to 2x 7W internal bass speakers in parallel or 1x 3.5W external bass speaker fitted via E405.

The 32" sets have internal centre and bass speakers. SW401 is fitted so the outputs of amplifiers I401 and I402 can be switched between the internal speakers and external speakers connected to E405.

The 36" sets have no facility for internal centre and bass speakers so SW401 is not fitted and the outputs of I401 and I402 are permanently connected to E405.

I401 is for the bass output.

I402 is for the centre channel.

I403 is for the rear right output.

I404 is for the rear left output.

Pin connection for TDA7482 (I401-404)

Pin 1 is the output which is a PWM (pulse width modulated) square wave with a peak to peak voltage that of the supply rails.

Pins 2 and 12 are connected together and are for the internal voltage regulators.

Pin 3 is the bootstrap connection.

Pin 4 is not connected.

Pin 5 is the feedback integration capacitor.

Pin 6 the resistor connected to this pin is used for setting the frequency at which the IC operates.

Pin 7 is ground.

Pin 8 is the signal negative supply.

Caution is required when checks are made as the metal tab of the IC is connected to pin 8, so the heat sinks are not connected to ground.

Pin 9 is the signal input.

Pin 10 controls the mute/standby functions, this pin controls the output state of the IC:

Voltage	Condition	Output at Pin1 (using oscilloscope)
0 to 1V	Standby	None
1.7V to 2.5V	Mute	Switching frequency square wave 50% duty cycle only
4V to 5V	Play	Switching frequency square wave with variable duty cycle (audio heard from speaker)

Pin 11 is the signal positive supply.

Pin 13 is the power output positive supply.

Pins 14 and 15 are the power output negative supply.

The front, centre, rear and bass channel amplifiers can be turned off independently by the user with software in the installation / speaker set up menu.

As the control of the amplifiers is the same for all the channels the centre channel will be used as an example:

When the set is turned on, the amplifiers are held in hardware mute by the microprocessor, by making the MUTE line high. This is applied to the base of Q412 via D406 and R426, which in turn holds the base of Q404 low. Q404 turns on pulling pin 10 of I402 low via D402, R420 (D402 and R420 are used to speed up the discharge of C419 at switch off) and R421.

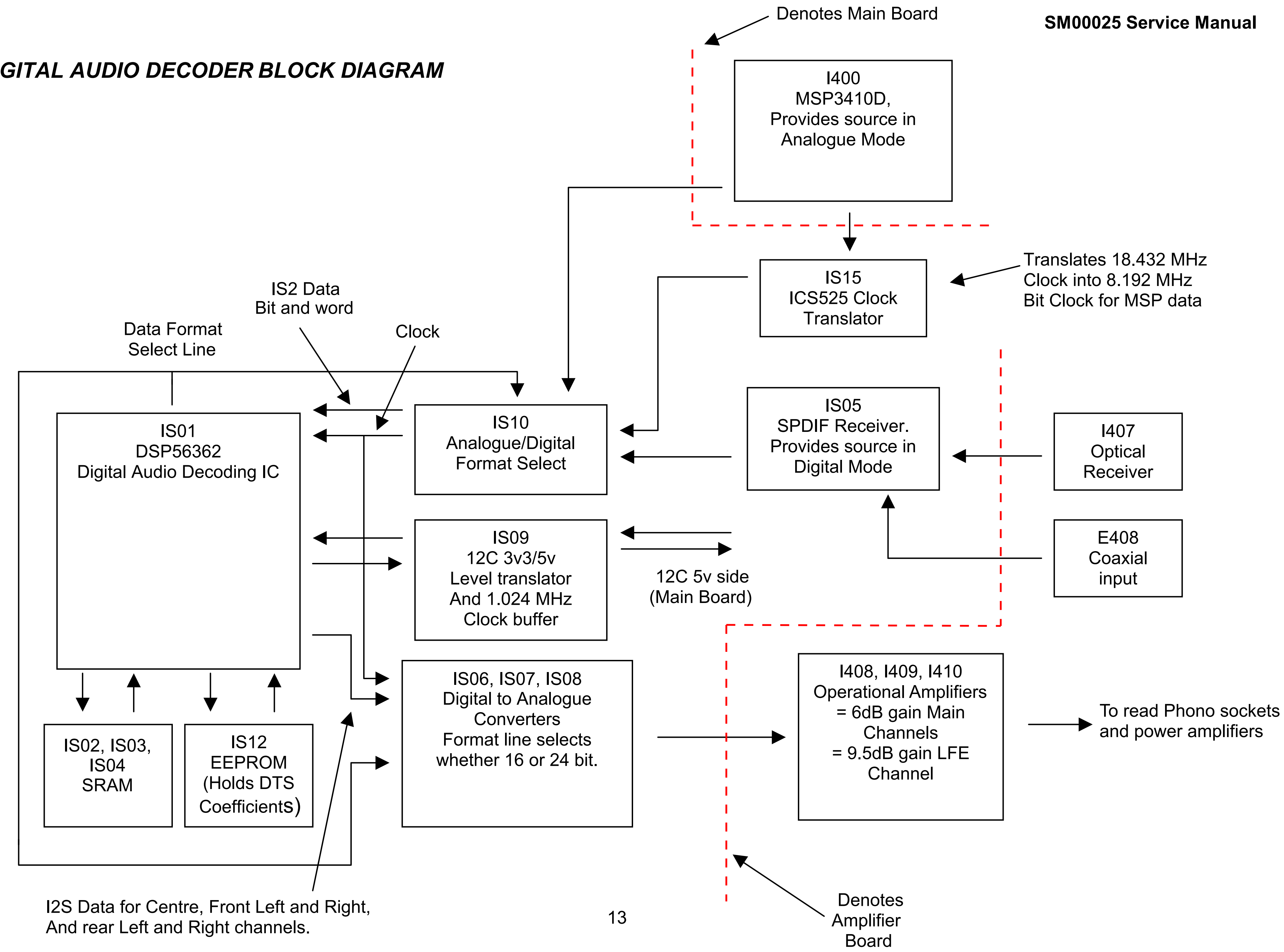
When the hardware mute is released pin 10 is pulled high (turning the amplifier on), via R419 clamped to 5.6V by Z402, R414 and R411. C419 is used to create a time constant to stop any pops when the amplifier is turned on.

When the centre channel is turned off using the software option the CENTRE OFF line is held low, turning off Q434, which in turn allows the base of Q403 to rise pulled high from the +17V via R447. Q403 turns on pulling pin 10 of I402 low via D402, R420 and R411.

Because internal centre and bass speakers are fitted to the 32" models and not the 36", SW401 is only fitted to the 32" so that external centre and bass speakers can be connected.

The 36" models have to have external speakers fitted.

DIGITAL AUDIO DECODER BLOCK DIAGRAM


Denotes Main Board
I400
MSP3410D,
Provides source in
Analogue Mode
IS15
ICS525 Clock
Translator
Translates 18.432 MHz
Clock into 8.192 MHz
Bit Clock for MSP data
IS2 Data
Bit and word
Data Format
Select Line
Clock
IS01
DSP56362
Digital Audio Decoding IC
IS10
Analogue/Digital
Format Select
IS05
SPDIF Receiver.
Provides source in
Digital Mode
I407
Optical
Receiver
E408
Coaxial
input
IS09
12C 3v3/5v
Level translator
And 1.024 MHz
Clock buffer
12C 5v side
(Main Board)
IS06, IS07, IS08
Digital to Analogue
Converters
Format line selects
whether 16 or 24 bit.
I408, I409, I410
Operational Amplifiers
= 6dB gain Main
Channels
= 9.5dB gain LFE
Channel
To read Phono sockets
and power amplifiers
IS02, IS03,
IS04
SRAM
IS12
EEPROM
(Holds DTS
Coefficients)
I2S Data for Centre, Front Left and Right,
And rear Left and Right channels.
Denotes
Amplifier
Board

1.14 DEFLECTION

1.14.1 100HZ HORIZONTAL DEFLECTION STAGE

The 2H output from UQ01 (the feature box) from pin 30 is fed via RZB7 to pin 24 of IZ04 TDA9330 the "HOP".

The horizontal drive is then output from pin 8 is passed through an emitter follower stage (QZ18) to the gate of Q701B. A MOSFET is used to sharpen the switching edges and reduce the temperature of the power transistor Q751. The drain of Q701B is fed from the +B via R701 and the primary of the drive transformer T702. The secondary of the transformer drives the base of the power transistor Q751, the collector of which is supplied from the +B via R751, L700 and the primary of the FBT. The emitter is connected to ground via R760 a 1Ohm 10W resistor (R760 should be kept away from Q751 heatsink to reduce heat transfer) which is a sense resistor for the protection circuit.

The capacitive divider network C717 and C708 produce a line pulse which is sampled by Z704 and clamped by D713 and D714 this is then returned to pin 13 of IZ04.

1.14.2 50HZ HORIZONTAL DEFLECTION STAGE

The HA OUT from pin 60 of I200 TDA9320 the "HIP" is fed via RZB7 to pin 24 of IZ04 TDA9330 the "HOP".

The horizontal drive is then output from pin 8 is fed to the base of Q701. The collector of Q701 is supplied from the +B via R701 and the primary of the drive transformer T702. The secondary of T702 drives the base of the power transistor Q751. The collector of Q751 is supplied from the +B via R751, L700 and the primary of the FBT. The emitter is connected to ground via R760 which is a sense resistor for the protection circuit.

The capacitive divider network C717 and C708 produce a line pulse which is sampled by Z704 and clamped by D713 and D714 this is then returned to pin 13 of IZ04.

1.14.3 VERTICAL DEFLECTION

On the 50Hz the vertical drive pulse come from pin 61 (VA OUT) of I200 and on the 100Hz it comes from pin 31 of UQ01. This is fed via RZB8 to pin 23 of IZ04. The vertical sawtooth waveforms are output from pins 1 and 2 of IZ04 and fed to pins 11 and 12 of I601 via RZ92 and RZ93. I601 (TDA8354) is the vertical output amplifier, it requires 2 supply voltages, approximately 14V to pins 4 and 10 to operate the IC and approximately 48V to pin 7 for the flyback pulse generator. The outputs are from pins 2 and 9 with the gain setting feedback resistors R602 and R603 connected to pin 5.

Z615 samples the flyback pulse which is then clamped by Z606 this generates the frame pulse used by the micro I001.

If vertical failure is detected I001 switches off to prevent damage to the tube.

1.14.4 EAST WEST CORRECTION

The east west parabola is output from pin 3 of IZ04 and fed to the gate of Q700 via RZ94. The drain of Q700 is connected to the centre of the diode modulator D706 and D707 via the east west injection coil L751.

1.15 MICRO-CONTROLLER SECTION

The main microcontroller on the A8/D8 chassis is located at I001 (ST92R195B). This is an 80-pin QFP (quad-flat package) that is surface mounted for compactness. This highly complex device controls many of the other integrated circuits via dedicated input/output lines or the I^2C bus. This device also generates the RGB signals for the on-screen display (OSD) menus and the Teletext. The device can acquire, decode and display the Teletext without the need for a separate IC. This microcontroller is ROM-less which results in the need of a separate memory device to store the program code necessary for operating the television. This memory device is located at I002 and is a multi-time programmable (MTP) or FLASH device. This allows the device to be re-programmed and in the future can even be re-programmed in the board without having to remove the back cabinet of the TV. The television stores all the necessary customer preferences and operating settings in an on-board EEPROM (E2). This device can hold 2Kb of information for storing the program information (frequency, name, AV setting, etc.), factory alignment settings (geometry, white balance, tuner AFC/AGC, etc.), service diagnostic errors and customer control settings (volume, brightness, contrast, etc.). This device communicates with the main microcontroller via the I^2C bus, even in the standby mode.

1.15.1 MAIN MICRO-CONTROLLER (I001)

The ST92R195B is an enhanced micro-controller based on the ST9+ instruction set from ST Microelectronics. It is capable of displaying menus and Teletext for 50Hz and 100Hz televisions. This device can acquire/decode and display pages of Teletext information in FLOF (FastText) and TOP (only in Germany/Switzerland/Austria) modes. The device operates from a single 4MHz crystal and a +5V supply. Dedicated address/data lines enable it to access 4Mbytes of address space, even though in this television it is accessing 128Kbytes (1Mbit). These address/data lines are connected to the EPROM/MTP/FLASH device which holds the instructions necessary for controlling the television, and on certain models to a 128K SRAM device used for 100 pages of Teletext storage.

External Memory Interface MMU Address Lines

Pins 1 (MMU0), 15 (MMU1) and 16 (MMU2) are used to access addresses above 64Kbytes. Normally pins 15 and 16 are not used when using a 128Kbyte EPROM/MTP device (MX26C1000APC) in position I002.

Pin 2 (MMU3) is used to select between either the EPROM/MTP/FLASH in position I002, or a future device that can be fitted in position I003. When this line is low, the device in position I002 is enabled (chip enable).

Pin 17 (MMU4) not used.

Pin 18 (MMU5) is not used.

External Memory Interface Control Lines

Pin 4 is the Data strobe line which is connected to the output enable input of the EPROM/MTP/FLASH (I002). When data is read from the EPROM/MTP/FLASH, this line is temporarily low.

Pin 8 is the Read/Write line for I002 and I003. Normally, this line is high and is low when writing data to the SRAM or FLASH device.

External Memory Interface Address Lines

Pins 3, 5, 6, 7, 13, 14 and 71 to 80 are the address lines needed to specify which location in a 64Kbyte page is needed to be accessed from the EPROM/MTP (I002) or SRAM (I003). Normally these lines will be changing state (0V to approx. +5V). By placing an oscilloscope on pin 12 of the EPROM/MTP (I002) it can be confirmed that the microcontroller is operating successfully. In this case, this line should be changing state very frequently.

External Memory Interface Data Lines

Pins 63 to 70 are the 8 data lines needed for receiving data from the EPROM/MTP (I002) or I003. Under normal circumstances these lines change from LOW (0V) to HIGH (approx. +5V).

Ground Connections

Pin 9 (GNDM) is the ground connection (0V) for the external memory interface. This should be free of noise to enable successful communications between the microcontroller and the EPROM/MTP (or SRAM).

Pin 35 (GND) is the digital ground connection (0V) for normal operation of the device.

Pin 62 (GNDA) is the analogue ground connection for the DAC and phase lock loops (PLL's).

Supply Connections

Pin 10 (VDDM) is the +5V supply for the external memory interface. Without this supply, the microcontroller cannot communicate with the EPROM/MTP (or SRAM).

Pin 34 (VDD) is the main digital supply voltage to the IC (5V 10% tolerance).

Pin 52 (VDDA) is the analogue supply voltage for the DAC's and PLL's (+5V). These connections are all joined together to the +5V standby rail of the television, ensuring that the microcontroller operates even in the standby state.

Crystal Oscillator Connections

Pin 11 is the 4MHz crystal oscillator input (OSCIN).

Pin 12 is the 4MHz crystal oscillator output (OSCOUT). By connecting a x100 scope probe to pin 11, it can be seen if a 4MHz sine wave is present at the oscillator input to the microcontroller.

Reset Connection

Pin 54 is the active low RESET input of the microcontroller. This input is normally high (approx. +5V) under operating conditions, but changes state when the standby +5V power supply is typically below +4.5V. In this circumstance, the reset IC (I021) pulls pin 54 low until the input of it is above +4.5V. The diode (D001) ensures that the capacitor (C015) discharges quickly when the standby supply falls, so that the reset operates quickly. The capacitor (C015) charges up slowly when the standby +5V supply is restored, ensuring that there is some hysteresis.

Infra-red (IR) Receiver Input

Pin 25 is the IR receiver's filtered output. This input from the IR receiver consists of PWM pulses between 0V and +5V which are decoded by the microcontroller into useful commands from the handset. When a valid command has been decoded, the Red LED on the front of the TV will briefly flash.

Horizontal and Vertical Synchronisation Connections

Pin 48 is the vertical synchronisation input from the deflection stage. This input is used to ensure that the OSD is displayed in a stable vertical position. When the TV is in the standby state, this input is normally low. The vertical input is triggered on the rising edge (positive polarity).

Pin 49 is the horizontal synchronisation input from the deflection stage. This input ensures that the OSD is displayed in stable horizontal position. When the TV is in the standby state, this input is normally low. This input is rising edge triggered (positive polarity).

General Input Connections:

Headphone Input

Pin 19 is used to detect if the headphone has been inserted into its socket. This input is normally HIGH (+5V) unless the headphone has been inserted, in which case it is near 0V. When the headphone is inserted, the headphone mode option is then available in the "Sound Mode" Menu and the loudspeakers (and internal sub-woofer if available) in the television are muted.

Protection Input

Pin 26 is used to determine if a protection fault has occurred on the chassis. This line is connected to the comparator outputs 1, 13 and 14 of I903 in the power supply. This line is normally high (approx. +5V) unless a fault has occurred, in which case it is near ground potential (0V).

Comparator output 1 monitors the +16V audio supply rail for over-current. If this rail is shorted, or draws too much current, then the comparator output (pin 1 of I903) will change state to 0V.

Comparator output 13 monitors the EHT voltage generated by the FBT in the deflection circuit. If this voltage is too high, then this output will be low to indicate that there is a problem with the deflection.

Comparator output 14 is connected to the secondary side of the deflection's line input transformer. It is primarily used to indicate whether too much current is being drawn from the line-input transformer and FBT.

Power-Good Input

Pin 27 is used to indicate if the power has been removed from the TV or whether a static discharge has occurred. This input is interrupt driven to react instantaneously to a falling edge (+5V -> 0V). Under this circumstance, the audio power amplifiers are muted and the television begins to power-down into standby. This input is derived from the comparator output (pin 2 of I903) in the power supply. This comparator provides an "early warning" indication that the primary supply has been removed or a static discharge event has occurred. Under a static-discharge condition, the TV will enter the standby condition temporarily before powering back up a few seconds later.

DTT Fan Fail Input

Pin 32 is used only on a D8 chassis fitted with a DTT module. It is used to indicate if a fault with the fan on the DTT unit has occurred (e.g. fan stuck). This input is normally HIGH (approx. +5V) unless a fault condition has been detected (0V).

Front Panel Buttons and SAV3 Socket Inputs

Pins 36 and 38 are 2 of the 4 ADC inputs of the microcontroller.

Pin 36 is connected to the Volume +/- buttons and the SAV3 (Hi-8) socket on the front panel of the TV. When the voltage on this pin is changed to a value in a certain window, the microcontroller will interpret it as either a volume +, volume -, volume +/- command and/or an SVHS Hi-8 connector was inserted into the Hi-8 socket.

Pin 38 is connected to the Program +/- and Menu buttons on the front panel of the TV. When the voltage on this pin is changed to a value in a certain window, the microcontroller will interpret it as either a program change or the menu button was pressed.

General Output Connections:

74HC595 Shift Register Outputs

Storage-Register Clock Output (RCLK)

Pin 20 of the microcontroller is connected to the rising edge (positive triggered) input (pin 12) of I006. This line is normally low when not communicating with the device or when shifting data into it. Once the full 8-bits have been shifted in, the RCLK line rises in order to latch the data to the device’s outputs.

EEPROM Write Enable Output

Pin 22 is the E2 write enable output line, which is connected to pin 7 of the EEPROM (E2). When this output is HIGH (approx. +5V), the E2 cannot be written to (write disable) but data from the device can be read. When this output is low (0V), then data can be written to the E2. This hardware line helps to protect the E2 from inadvertent write operations, which could occur under abnormal circumstances.

On/Off Output

Pin 43 is the On/Off line which turns On (LOW) /Off (HIGH) the secondary supplies (+B, +16V audio rail, +8V and +5V). The standby +5V and+10V rails are unaffected when this output is HIGH (TV in the standby state). Under normal operating conditions, this output will be low when the TV is NOT in the standby condition.

On/Off 2 Output

Pin 29 is the On/Off 2 line which turns On (LOW) / Off (HIGH) the DTT/ASW sub-power supply.

I^{2}C Disable Output

Pin 33 is the I^{2}C disable output which prevents the main chassis I^{2}C bus from being connected to the I^{2}C bus of the microcontroller (I001) and E2 (I002). This line is normally HIGH when the TV is in the standby state. This output is inverted using the 74HC04 hex inverter IC (I004) and in connected to pins 5 and 6 of I007. In the standby condition, pins 5 and 6 of I007 (74HC4066) are low and the M.SDA and M.SCL (microcontroller) lines are disconnected from the SDA and SCL (main chassis) I^{2}C lines. When writing to the E2, the I^{2}C disable output is also pulled high, to ensure that successful writing of the data has occurred (e.g. to log fault diagnostics when the TV fails to power-up and the main chassis I^{2}C bus is low).

Scart Disable Output

Pin 39 is used to route the AV/diagnostic link between pin 10 of AV1 or pin 10 of AV2

Mute Output

Pin 40 is the mute output for the on-board audio amplifiers. This output is HIGH when the amplifiers are in the mute condition (e.g. Standby). If the user has chosen to use the internal speakers, then under normal operating conditions, this output will be LOW. When powering down, this output will quickly rise to mute the speakers, to prevent any unwanted ‘popping’ noises from being heard.

Green LED Output

Pin 41 is the green LED output, which is only used on the digital chassis fitted with a DTT module. This output is high when the green led is ON. When the DTT module is in the partial standby state or when recording a digital terrestrial program, then this LED will be ON and will be mixed with the red LED to produce an amber colour. When the DTT module is connected via the telephone line and receives mail, then this LED will flash periodically to indicate this condition.

When the TV first has power applied to it, then the green LED will be ON. Soon after, though, this LED should extinguish to indicate that the TV is operating correctly. NOTE: This is one of the easiest ways to check that the microcontroller is running the program code correctly in the EPROM/MTP. If the green led remains ON, then the microcontroller or EPROM/MTP has a fault preventing the code from being executed correctly.

Red LED Output

Pin 42 is the red LED output, which is used to indicate the standby state and when an IR command has been successfully received and decoded. When the TV is in the standby state, this output will be HIGH to ensure that the red LED is brightly lit. When the TV is not in standby, then this output will be low, but the red LED will remain dimly lit through resistor R081. When an IR command has been successfully received, then the LED will flash briefly, to inform the user that the button on the handset was pressed correctly.

I^{2}C Connections

Pin 23 is the I^{2}C bus data input/output for transferring data between other I^{2}C peripherals/devices. This line is only connected to the EEPROM (I005) when in the standby state or when writing to the EEPROM. This line is constantly active when the TV is powered up and normally changes state between (+5V and 0V).

Pin 24 is the I^2C bus clock output for clocking the data to other I^2C peripherals/devices. The clock line is also disconnected from the main chassis when in the standby state or when writing to the EEPROM. This line oscillates at a frequency around 90KHz

RS232 Connections

Pin 30 is the RS232 Transmit line from the microcontroller. It is connected to pin 3 of connector P001 for the DTT module (only on D8 chassis).

Pin 37 is the RS232 Receive line for the microcontroller. It is connected to pin 4 of connector P001 for the DTT unit (only on D8 chassis).

RGB Connections

Pin 44 is the OSD/Teletext RGB blanking signal necessary for allowing insertion of the OSD/Teletext onto the picture. When this output is high (approx. +5v), then the RGB signal will be superimposed onto the current picture.

Pin 45 is the OSD blue signal necessary for displaying BLUE colors for the OSD and Teletext.

Pin 46 is the OSD green signal necessary for displaying GREEN colors for the OSD and Teletext.

Pin 47 is the OSD red signal necessary for displaying RED colors for the OSD and Teletext.

CVBS Connections

Pin 60 is the Composite Video signal input for VPS and WSS slicing. It is normally AC coupled and internally clamped to ensure reliable operation. VPS (video programming system) is necessary when auto-sorting programs in Germany/Austria/Switzerland. WSS (wide-screen signaling) is used to indicate the aspect ratio of the incoming signal. The TV can then use this information to display the picture in the correct format.

Pin 61 is the Composite Video signal input for Teletext acquisition and decoding and also for sync extraction, necessary for obtaining the correct line timings for slicing the Teletext information and VPS/WSS information.

1.15.2 EPROM/MTP/FLASH (I002)

The device located in position I002 is used to store the program code needed by the microcontroller to operate the television correctly. The device currently used on the A8/D8 chassis can hold 128Kbytes of information (1Mbit). This device also holds any initialisation data to be downloaded to an EEPROM. When a blank EEPROM is fitted, the initialisation data is automatically downloaded to it when power is applied to the chassis.

Supply/Ground Connections

Pins 32 and 16 are the +5V supply and ground connections respectively. The supply voltage of +5V is always present even when the TV is in the standby state.

Address Connections

Pins 2 to 12, 23 and 25 to 29 are the 17 address lines needed to access the full 128Kbytes of 8-bit data inside the device. These lines are connected directly with the microcontroller so that it can request data from the MTP when operating. An oscilloscope can be used to check pin 12 of the MTP to check whether the microcontroller is running correctly and accessing the MTP. This pin should be oscillating at a frequency of around 2MHz and is a non-periodic square waveform.

Data Connections

Pins 13 to 15 and 17 to 21 are the 8 data lines needed to transmit a byte at a time to the microcontroller. These outputs are normally tri-state and are high-impedance when the output enable pin 24 of the MTP is HIGH. When the output enable pin is low, the data from the required address will be output on these pins.

Output Enable Connection

Pin 24 is the output enable active low input used to control the logical state of the data lines. When this pin is HIGH, the data lines are in the high impedance condition and no data is present on these pins. When the output enable input it LOW, the data lines are active and output the addressed data, This line is connected to the data strobe output of the microcontroller to ensure correct operation/timings.

Chip Enable Connection

Pin 22 is the chip enable active low input used to select the device. Normally, this input is low to enable the device. However, the device can be placed in a standby state when accessing a future SRAM in position I003. The MMU3 line from the microcontroller is used to select either the SRAM or the MTP. When no SRAM is fitted, the chip enable pin is always low.

Miscellaneous

Pin 1 (VPP) is the programming voltage input pin (+12.75V needed) used to re-program the device when placed in a special programmer. This pin is always tied to the +5V standby supply, to ensure that the device can never be re-programmed inside the television chassis.

Pin 30 is not used in this device. However, it is still connected to the MMU1 line from the microcontroller for use with larger size MTP's/EPROM's. This line can be used to access a further 128Kbytes if such a device was fitted.

Pin 31 is the active-low programming enable pin that is used to re-program and erase the device. This pin is normally at +5V but pulses to ground when data is written to this device.

1.15.3 SRAM (I003)

The position I003 is used to hold an SRAM for Teletext page storage and memory storage. A 128Kbyte device is situated here to allow 100 Teletext pages to be acquired and stored for immediate fast access to them. The SRAM is connected to the microcontroller's address and data lines, which are shared with the EPROM/MTP in position I002.

Supply/Ground Connections

Pins 32 and 16 are the +5V supply and ground connections respectively. This device always has +5V connected to it, even when the TV is in the standby state.

Address Line Connections

Pins 2 to 12, 23, 31 and 25 to 28 are the address lines needed to access the 128Kbyte of data by the microcontroller.

Data Line Connections

Pins 13 to 15 and 17 to 21 are the 8-bit data lines needed to receive/transmit a byte of data at a time to/from the microcontroller.

Chip Enable Connections

Pins 22 and 30 are 2 chip enable inputs that need to be LOW and HIGH respectively for the 128Kbyte device to operate. If either pin 22 is HIGH or pin 30 is LOW, then the device enters a standby state whereby its power consumption is dramatically reduced (10uW). The MMU3 output pin from the microcontroller (pin 2) is used to select the SRAM when it is HIGH. If this pin is low, then the MTP/EPROM in position I002 is selected instead.

Write Enable Connections

Pin 29 is the active-low write enable input used to enable data to be stored inside the device. This pin is connected to the read/write line of the microcontroller for synchronisation purposes.

1.15.4 74HC04 HEX INVERTER (I004)

The 14-pin IC in position I004 is a high speed CMOS hex inverter used to invert digital signals. The package consists of 6 inverters, but only 4 are used in this application.

Supply/Ground Connections

Pins 14 and 7 are the +5V and 0V supply connections respectively. This device always has +5V supplied to it, even when the TV is in the standby state. Capacitor C023 is connected across the supply terminal for de-coupling.

Chip Enable Connection

Pin 1 is connected to the MMU3 output from the microcontroller and is used to select either the MTP or the SRAM. This signal is inverted and output from pin 2 that is then connected to the active low chip enable input (pin 22) of the SRAM. In this way, only one chip enable line from the microcontroller needs to be used to enable the SRAM.

AVTX Disable Connection

Pin 3 is the AV/diagnostic transmit line from I001 pin 21. This input is inverted and is outputted at pin 4, before being connected to pins 12 & 13 of the analogue switch (I008).

I^{2}C Disable Connection

Pin 5 is the I^{2}C disable input from pin 33 of the microcontroller. This signal is inverted and output at pin 6 to pins 5 & 6 of the analogue switch (I007). When the microcontroller is in the reset condition, or when the TV is in the standby state, the I^{2}C disable line is HIGH. This signal must be inverted to disable the microcontroller's I^{2}C bus from the I^{2}C bus of the rest of the chassis.

SCART Select Connection

Pin 13 is the SCART select input from pin 39 of the microcontroller. This input is inverted and output at pin 12, which is then connected to pins 12 and 13 of the analogue switch (I007).

1.15.5 EEPROM (I005)

The ST24C16 EEPROM, or E2 as it is commonly known, is a 16Kbit (2Kbyte) device that holds non-volatile data when power is removed from the TV. This device can hold information for 100 programs, such as the name, frequency, standard, AV setting, speaker language setting and Teletext favourite pages. The EEPROM also holds diagnostic fault codes used to help identify previous faults with the chassis (see separate section that deals explicitly with this). The E2 also holds factory aligned parameters, such as the geometry, white balance, tuner AFC/AGC, model type, cathode level, etc. The E2 also holds the user's preferential settings, such as the volume, balance, contrast, brightness, etc. Data is written to/read from the device using the standard Philips I^{2}C protocols.

Supply/Ground Connections

Pins 8 and 4 are the +5V supply and ground (0V) connections respectively. The EEPROM is powered from the +5V standby rail so that it always has power to it, even when the TV is in standby.

I^{2}C Connections

Pin 5 is the I^{2}C Data line needed to transfer serial data between the microcontroller and itself. Data is changed when the clock line is low and latched on the rising edge of the I^{2}C clock.

Pin 6 is the I^{2}C clock line needed to synchronise the I^{2}C data transfer. 9 clock pulses are needed for the 8-bit data and an acknowledge bit. The I^{2}C master clock originates from the microcontroller and operates at a frequency around 100KHz.

Address Connections

Pins 1 to 3 are the address lines used to select the I^{2}C slave address of the device. On the ST24C16 device, these lines must be connected to ground in order to access the device properly.

Write Disable Connection

Pin 7 is the I^{2}C write enable/disable input. When this input is HIGH (+5V), all I^{2}C writes to the device are denied. When the pin is pulled low by the microcontroller (pin 22 E2RD), data can be written to the device. In this manner, inadvertent write operations can prevent the I^{2}C data from being corrupted.

1.15.6 74HC595 SHIFT REGISTER (I006)

The 74HC595 is a 16-pin high-speed CMOS 8-bit shift register used for additional output port capability on the A8/D8 chassis. 8-bit data is serially shifted into the device and then latched to the outputs when so desired. These outputs are not used when the TV is in the standby state.

Supply/Ground Connections

Pins 16 and 8 are the +5V supply and 0V ground connections respectively. This device has +5V supplied to it, even when the TV is in the standby state. Capacitor C024 is used to de-couple the supply.

VM On/Off Output Connection

Pin 1 is used to turn On (LOW) or Off (HIGH) the VM (velocity modulation) circuit of some high-end chassis. This improves the transition from black to white (and vice versa) areas of the picture to sharpen them up. This is particularly noticeable at the outer areas of the CRT. This output pin is connected to the +5V signal supply and so is left floating when the TV is in the standby state. The diode, D008, prevents any leakage current from flowing from pin 1 to the VM circuitry when the TV is in the standby state.

On sets with the auto widescreen device fitted on the signal sub PCB this line pulses low to communicate the autowidescreen device.

Mute 2 Output Connection

Pin 2 is used to switch the ASW amplifier into standby (LOW) or operating mode (HIGH). This pin is also used to step down the +16V supply at the rear of the TV to mute an optional console/speaker system connected to the +16V phono connector, when power is removed from the TV.

Compress Output Connection

Pin 3 is the compress relay enable (HIGH) or disable (LOW) control. This output is high when a widescreen TV is in 4:3 aspect ratio, and is low in all other modes. In 4:3 mode, black side panels are observed either side the central picture.

External Blanking Output Connection

Pin 4 is the external RGB blanking output, needed to switch the external blanking input (pin 39) of the HIP (TDA9320) into full-screen blanking mode. This mode is activated when the user selects "RGB" from the possible AV modes. In this instance, the line is HIGH causing the RGB signals on pins 36 to 38 of I200 to have precedence over the picture.

MSP Reset Output Connection

Pin 5 is the MSP3410D reset line that is low when the MSP is being reset. This line is normally HIGH (+5V) when the TV is operating correctly. When the TV is in the standby state, this line is low, as there is no +5V signal supply to pull the line up through resistor R044.

Mute3 Output Connection

Pin 6 is the Mute3 output needed to mute the ASW amplifier. When this line is HIGH, the internal sub-woofer (optional on some models) is muted. This occurs if the user has disabled the internal speakers from the speaker configuration menu, headphones are inserted into the TV, or when the TV is powered off.

DTT Reset Output Connection

This pin is connected to pin 1 of the DTT connector (P001) and switches low to reset the DTT module.

Shift Register Clear Input (SCLR)

Pin 10 is an active low input necessary for clearing the shift register’s data on power-up.

Shift Register Clock Input (SCK)

Pin 11 is the shift register clock input necessary for clocking the data into the device. Each bit of data is latched into the device, on the rising edge of the clock. This clock originates from SCL I^{2}C line.

Register Clock Input (RCK)

Pin 12 is the register clock input necessary for latching the data to the output pins. On the rising edge of this pin, all 8 latched bits are transferred to the output pins.

Output Enable Input (G)

Pin 13 is an active low input necessary for enabling the output ports. This pin is always connected to ground to enable the outputs.

Shift Data Input

Pin 14 is the shift data input necessary for transferring the 8 data bits into the device. When this line is HIGH, a logical ‘1’ is latched into the device on the rising edge of SCK. When this line is low during the rising edge of SCK, a logical ‘0’ is stored instead.

1.15.7 74HC4066 ANALOGUE SWITCH (I007)

The 74HC4066 is a 14-pin high speed CMOS quad bilateral switch. It is used primarily for connecting/disconnecting signals when out of/in the standby state.

Supply/Ground Connections

Pins 14 and 7 are the +5V supply and 0V ground connections respectively. This device is always powered up, even when then television is in the standby state. Capacitor C025 ensures that the supplies are properly de-coupled.

AVLINK Connections

Pin 1 and 11 are the AV link line to from the microcontroller (pins 21 and 31)

RXD Connections

When pin 13 is high, this is connected to pin 2 and AV2 pin 10

When pin 12 is high, this is connected to pin 10 and AV1 pin 10

I^{2}C Connections:

I^{2}C Clock Connection

Pin 8 is the I^{2}C master clock input from the microcontroller (pin 24). When pin 6 of I007 is HIGH, this line is connected to pin 9, which enables the microcontroller to communicate with other I^{2}C devices on the chassis. Pin 6 is normally LOW when the TV is in the standby state, or when power is first applied to the chassis.

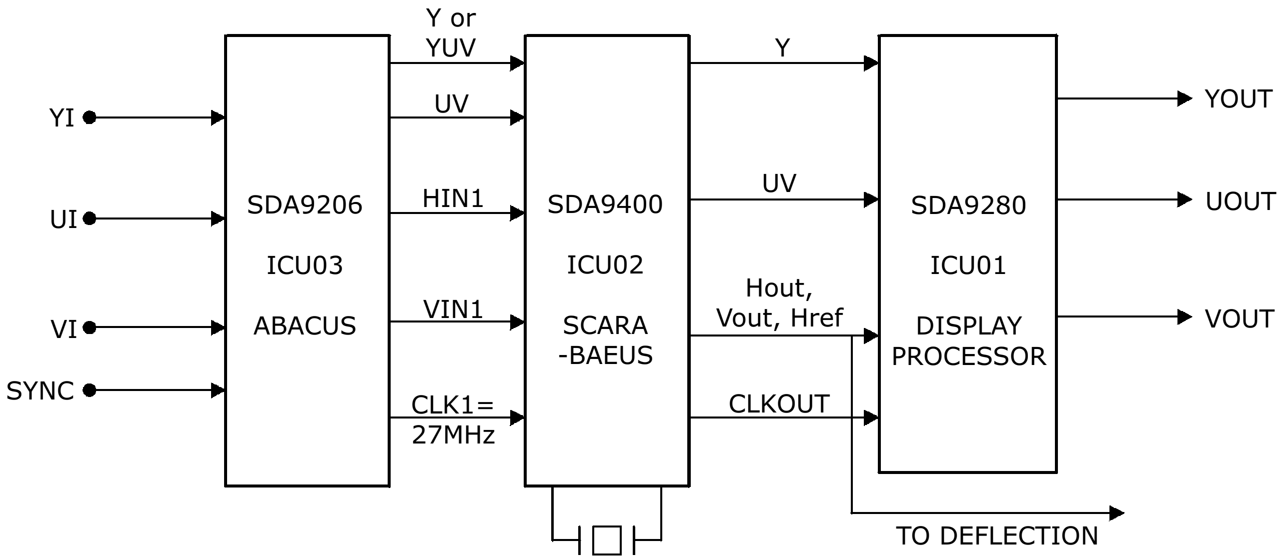
I^2C Data Connection

Pin 4 is the I^2C data input from the microcontroller (pin 23). When pin 5 of I007 is HIGH, this line is connected to pin 3, which enables the microcontroller to communicate with other I^2C devices on the chassis. Pin 5 is normally LOW when the TV is in the standby state, or when power is first applied to the chassis.

1.16 MULTIPICTURE FUNCTION

The multi-picture option scans various channels displaying in a selection of box sizes on-screen. For multi-picture operation the cross button ⊗ should be pressed. An adjustable scanning speed (9 steps), with two scan modes (multi and single) and a choice of three display types may be chosen. If the cross button ⊗ is pressed in service mode, the multi-picture function will briefly become unstable due to loss of sync from an initial forced no sync condition. When exiting service mode into user mode a blanking condition for the initial unstable capture times is implemented.

HIGH END FEATURE BOX:


YI
UI
VI
SYNC
SDA9206
ICU03
ABACUS
Y or YUV
UV
HIN1
VIN1
CLK1= 27MHz
SDA9400
ICU02
SCARA -BAEUS
Y
UV
Hout, Vout, Href
CLKOUT
SDA9280
ICU01
DISPLAY PROCESSOR
YOUT
UOUT
VOUT
TO DEFLECTION

1.17 AUTOWIDESCREEN

Autowidescreen section of the A8 Mark II chassis

The autowidescreen microcontroller is located on the signal processing board of the mark II chassis labelled as IZ02. (AT90S1200)

This device is used to differentiate between a 4:3, 14:9 and 16:9 picture by means of the horizontal and vertical sync. pulses and the luminance signal. To provide the luminance in a form that is usable for the micro, the luminance of the signal is compared with a reference voltage which is controlled by the micro, with three output pins controlling the reference voltage at pin 5 of IZ03. The luminance is connected to pin 6 of IZ03, and the output, pin 7, is pulled up by RZ68 and connected back to the micro on pin 8.

1.17.1 AUTOWIDESCREEN DETECTION MICRO (IZ02)

This micro is an ATMEL AT90S1200 microcontroller. The main task of this micro is to detect black bands at the top and bottom of the picture. Using the size of the bands it can determine whether the picture is of a 4:3, 14:9 or 16:9 aspect ratio.

Power connections

Pin 20 (VCC) is the supply voltage to the IC. The device will tolerate a range of 2.7 - 6.0V, but uses the 5V supply to the board.

Pin 10 (GND) is the ground connection for the chip.

Crystal connections

Pin 4 (XTAL2) is the crystal oscillator output.

Pin 5 (XTAL1) is the crystal oscillator input. This pin should oscillate at 12 MHz when the set is out of standby.

I^{2}C and general input/output connections

Pin 2 (PD0) is used as an I^{2}C data line. This is connected to the main I^{2}C line via RZ79.

Pin 9 (PD5) is used as an I^{2}C clock line. This is connected to the main I^{2}C line via RZ80.

Pin 6 (PD2) is used as an I^{2}C attention line. The main micro pulls this low when it is necessary to communicate with this micro. The main micro uses this line as a VM line if this micro is not detected.

Pin 7 (PD4) is the velocity modulation (VM) out line. Link KZ05 connects these two together allowing the main micro to use the VM line if there is no autowidescreen micro. The main micro sends the requested state of this line via the I^{2}C bus.

Sync and luminance comparator connections

Pin 11 (PD6) connects to the vertical sync. This signal is taken from pin 61 of the input processor I200.

Pin 12 (PB0/AIN0) connects to the reference voltage.

Pin 13 (PB1/AIN1) connects to the horizontal sync. This signal is taken from pin 60 of I200 – the input processor TDA9320.

Pin 8 (PD4) connects to the output of comparator IZ03.

Pin 15 (PB3) is the least significant pin controlling the reference voltage. It is connected via RZ63.

Pin 16 (PB4) is the second pin controlling the reference voltage. It is connected via RZ70.

Pin 17 (PB5) is the most significant pin controlling the reference voltage. It is connected via RZ71.

Other pins

Pins 1, 17, 18 and 19 are used for programming the device while in circuit. These connect to connectors PZ01 and PZ07.

Pins 3 and 14 are currently unused.

2 SERVICE

2.1 BOARD ADJUSTMEMT

2.1.1 FOR SIGNAL

PREPARATION ADJUSTMENT

+B adj. Set R982 to centre position

Set screen pot T701 (FBT) fully anti-clockwise

Turn on set. Adjust +B to approximately 152V. (Pre adjustment only)

If flaring is observed, adjust L501 until a clean video signal is seen on the oscilloscope video out port.

For Models with a flash device fitted, ensure the service information reads:
`FLASH: x.x` instead of `Code: x.x` for the software version.

The batch and serial number must be programmed into the EEPROM at locations: 0635-0644 inclusive using the diagnostic interface. The data is to be programmed in ASCII format.

STANDARD AFC ALIGNMENT

To reduce the influence of circuit temperature drift, let the television warm up by leaving it operating normally for more than two minutes.

Receive a 'PAL I' signals by selecting program 3 via the remote control handset.

Receive a signal level of +60 dBmV at 623.25MHz (CH40) by **direct frequency entry** under the CH option.

Set AFC offset (in service – options) to the centre position.

In the tuner menu select standard IF AFC and press either '<' or '>' on the remote control to activate the automatic AFC setting procedure. If the indicator goes either end of spectrum, then returns to the centre, adjust L201 one turn and then return to step 3, continue this until the indicator bar no longer jumps back to the centre.

L' AFC ALIGNMENT (for export models only)

To reduce the influence of circuit temperature drift, let the television warm up by leaving it operating normally for more than two minutes.

Receive an L' signals by selecting **program 14** via the remote control handset.

Receive a signal level of +60 dBmV at 63.75MHz (CH4) by **direct frequency entry** under the CH option.

In the tuner menu select L' IF AFC and press '<' or '>' on the remote control.

If the bar goes to either end then returns to centre, adjust L201 one turn and then return to step 3, continue this until the indicator bar no longer jumps back to the centre.

Because the set up procedures are interactive, it is necessary to repeat all procedures from **"STANDARD AFC ALIGNMENT"** above until no adjustment of L201 is required.

AGC ALIGNMENT

To reduce the influence of circuit temperature drift, let the television warm up by leaving it operating normally for more than two minutes.

Receive channel 40 (623.25MHz) at +60dBmV.

Adjust AGC takeover option (Service >> Tuner) to maximum:

.00 (XX)	Max. AGC Voltage

(xx denotes current AGC voltage in hexadecimal steps form.)

Reduce AGC take-over option, until reading in brackets moves by one step.

XX (one step deviation)	Take-over Point

(xx. denotes number of AGC steps from max. AGC.)

Note:
MES must check input signal level everyday.

2.1.2 POWER AND DEFLECTION ADJUSTMENT

+B VOLTAGE ADJUSTMENT

AC input voltage = 230± 5V / 50Hz.

Turn +B voltage (R982) to mid-point (if pre-adjustment not done).

Receive Philips circuit pattern. Switch on chassis and set the brightness and contrast to maximum.

After applying heat, run for 1 minute or more then turn R982 gradually and adjust +B (re-check after 30 secs).

Measuring point:	+B voltage Gnd	C958 + side C958 - side

Set the value of +B voltage to the value shown in the table below.

MODEL	+B VOLTAGE (V)
All A8MkII 50Hz	151V ±0.2V (except 28”)
All A8MkII 100Hz	147V ±0.2V (except 28”)
All D8MkII 100Hz	147V ±0.2V (except 28”)
All A8MKII 28”	141V ±0.2V

Check + B voltage in standby > 145V and < 160V.

Short circuit test (all rails). PSU should go into standby/reset/lockup (supply may have to be removed to restart). Audio rail should be tested, Q921 source to 0V.

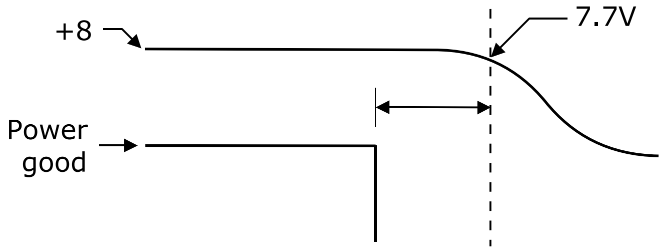
	Min Load	Max Load
+8V = 8V ± 5%	0.3A	0.8A
+5V = 5V ± 5%	0.3A	0.8A
+16V = 16V (+3V, -1V)	0A	1.6A
+16V (Phono) = +16V (+3V, -1V)	0A	200mA
+B	0.2A	0.8A

POWER GOOD LINE

Set picture to same conditions as stated in earlier sections.

Measure I903 pin 2. Should be HI, if LOW then cut R962 (if fitted). If HI but no power, down timing (see below) then cut R955 (if fitted).

Check power down logic timing (>30mS, < 300mS).



After setting Power Good, check operation at 200VAC mains

PRIMARY CURRENT LIMIT

(Pre-set R980 to mid point)

Rail	Trip Load	Check Load	Trip Power	Check Power
+B	1.3ADC	1.24A	196W	186W
+16V	2.24ADC	1.65A	36W	26W
+11V (+5, +8)	1.60A	1.60A	18W	18W
TOTAL Wattage			250W	230W

In standby apply full load +40%, to the +B & audio/+11V rails (dynamic load) as table above.

Adjust R980 until set trips out.

In standby, apply check load. PSU should not trip.

STANDBY OPERATION CHECK

Check all rails (except +B and standby +5V) go to 0V.

Check +B does not rise above 160V

Check operation frequency falls to < 40KHz, >20KHz.

Check input power is < 5.25W.

GENERAL SAFETY CHECKS

High voltage BEAB test to confirm components across barrier (including sub board).

Deg relay insertion orientation test (relay can be fitted inverted on main and sub PSU console stand).
+ Job instruction to show orientation of relay.

SUB BOARD PSU CHECK

Short circuit test (all rails)

Output voltage test (all rails), see table.

Standby operation. All rails should be off. +10V remains to supply sub PSU & opto.

Full load operation check.

RAIL	Audio (A8)	DTT (D8)
3.3V	Not Used	2.7A
5.1V	Not Used	1.5A
9V	Not Used	400mA
12V	Not Used	10mA
+17V	2.5A	2.5A
-17V	2.5A	2.5A
30V	Not Used	10mA

DTT +5V SETTING

Set VR1 to approx. centre position (10KΩ).

Turn power on applying external load, see table.

Adjust VR1 making sure +5.2V rail is within ± 0.05V.

SUB-BOARD MUST BE BEAB TESTED IN A SET OR CONSOLE STAND

Adjust R9055 until +17V is across C9046 at full load of 2.5A. During no load condition 17.5 to 18V should appear across C9046.

HIGH VOLTAGE LIMITER CIRCUIT CHECK

Mount the PCB to the set and adjust normally.

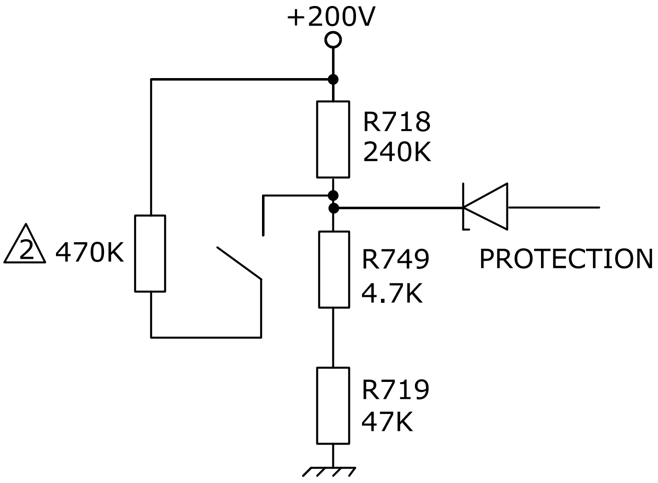
Receive the circle test pattern.

Set the Contrast and brightness to maximum.

Add R=470KW in parallel with R718 and R718A.

Check that picture and sound disappear when R is added.

High voltage limiter circuit jig:



ANODE/FOCUS SHORT-CIRCUIT TEST PROTECTION CIRCUIT CHECK

Add a DC voltage to R760 until set trips. The DC level should be equivalent to

DC level = 1.7 * (+B current peak value)

0.6 VDC R760 SET **SHOULD NOT** TRIP
1.6 VDC R760 SET **SHOULD** TRIP

FINAL ANODE VOLTAGE LEVEL CHECK

Check on all 100Hz models that the final anode voltage does not exceed the voltages listed below.

28” 16:9	**33KV**
32” 16:9	**33.5KV**
36” 16:9	**34KV**

This test should be carried out in AV Mode (No signal).

2.1.3 FEATURE BOX (100HZ/PROGRESSIVE SCAN)

+5V & +8V SHORT CIRCUIT CHECK USING FEATURE BOX BOARD

Measure the resistance between 5V (EU11, pin1) and GND (EU11, pin3) using multi-meter. If the meter shows 62.5W ± 4W, The FEATURE BOX is OK.

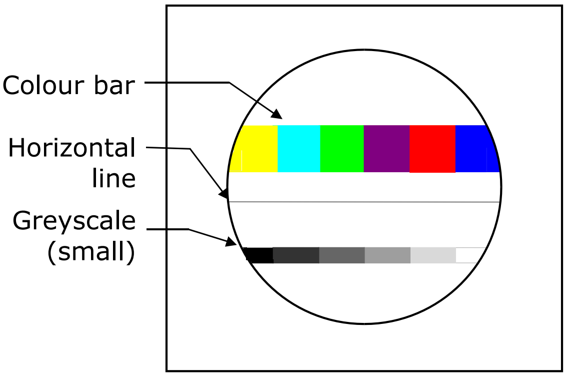
Measure the resistance between 8V (EU11, pin6) and GND (EU11, pin3) using multi-meter. If the meter shows 1.29KW ± 0.1KW, The FEATURE BOX is OK.

FEATURE BOX OPERATION CHECK

Fit FEATURE BOX into main board.

Receiving circle test pattern (PAL), check the picture quality.

Check: Horizontal line is stable (see horizontal line). White part of picture is pure white (see diagram).



Check the Progressive Scan/100Hz operation by handset.

Change sharpness, CTI, compression (14:9, 4:3 & zoom), noise reduction (Auto, low, mid & high) by handset. Check the total performance. Whenever digital noise appears on the picture, or mis-operation occurs, reject the feature box.

Receive an NTSC signal and repeat **"FEATURE BOX OPERATION CHECK"** section above again.

2.2 FINAL ALIGNMENT (by Software)

2.2.1 PICTURE POSITION/SHAPE

HORIZONTAL PHASE
VERTICAL CENTRE
VERTICAL AMPLITUDE

Wait 5 minutes minimum, after switching on the mains before adjustment.

Receive circle test pattern.

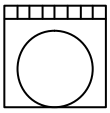
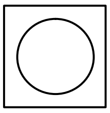
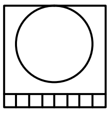
Set Brightness and Contrast to maximum.

The set should face North or South.

AC input should be 230 ±5V 50Hz.

Adjust software control (using PC / HAND SET)

Adjust control so that the centre of the picture is as in the diagram below.

	Upper: Extends Lower: Shrinks	Standard	Upper: Shrinks Lower: Extends
Picture Condition			
Size	Adjust until upper castillations disappear	Adjust until both castillations disappear	Adjust until lower castillations disappear

Note:
The picture should be exaggerated as to create a barrel type picture at the vertical edges. The compensation to achieve this barrel picture should be 3 steps passed the straight vertical edge position. This is to compensate for the pincushion effect noticeable on OSDs.

TILT
PARABOLA
WIDTH

Allow 5 minutes warm up time before adjustment.

Receive circle test pattern.

Set Brightness and Contrast to nominal.

The set should face North or South.

AC input source should be 230V ± 5V 50Hz.

Adjust software so that the vertical lines at the outside edges of the screen are adjusted to be roughly vertical.

Adjust the software so that the (approximately) vertical lines at the sides of the screen are adjusted as vertical as the centre of the screen.

Adjust the software so that the castillations at the sides of the picture are not quite visible. Reduce the brightness and contrast to make sure that the picture width has not reduced so that you can see beyond the castillations. You may have to repeat stages 6 and 7 again.

Note:
For all 16:9 receivers the picture should be first set up in 16:9 mode, then final adjustment for parabola and corner correction only to be carried out in 4:3 mode.

BOW (only for N2 version TDA9330 – IZ04)
U CORNER
L CORNER
TIMING

Allow 5 minutes warm up time before adjustment.

Receive circle test pattern

Set Brightness and Contrast to nominal.

The set should face North or South.

AC input source should be 230 ±5V 50Hz.

Select SERVICE »» HORIZONTAL and scroll down to BOW.

Adjust BOW in software menu until vertical lines across the entire screen are approximately straight and vertical.

Scroll up and adjust U CORNER until vertical lines at top corners of the screen are vertical.

Adjust L CORNER until vertical lines at bottom of the screen are vertical.

If there is any ‘fold over’ at right hand edge of the screen, increase TIMING until it disappears.

Note: (U CORNER and L CORNER adjustment)
Best results may be obtained when altered in conjunction with PARABOLA.

2.2.2 FOCUS ADJUSTMENT

Receive circle test pattern.

Adjust after Horizontal/Vertical has been adjusted.

Switch the received signal to the crosshatch signal.

Turn the static focus pot (middle pot) gradually clockwise starting from the full anti-clockwise position. The vertical line furthest to the right should be focused for the best result (Contrast – Max, Brightness – nominal).

Turn the dynamic focus pot (top pot) gradually clockwise starting from the full anti-clockwise position. Focus of the horizontal line at the top of the picture for the best results (Contrast – Max, Brightness – nominal).

2.2.3 CUT-OFF ADJUSTMENT

Rough Adjustment:

Select AV mode without signal.

- Turn Screen pot of FBT (T701) until flyback lines disappear.

Fine Adjustment.

Select AV mode without signal.

In the White Point service menu there is an indicator at the bottom, representing the status of the Auto Cut-off loop.

0+ or **i-** or **0-**

Adjust Screen pot until indicator displays ‘i-’.

2.2.4 RGB SHIFT

Receive RGB signal from SCART.

SERVICE »» HORIZONTAL »» RGB SHIFT by handset.

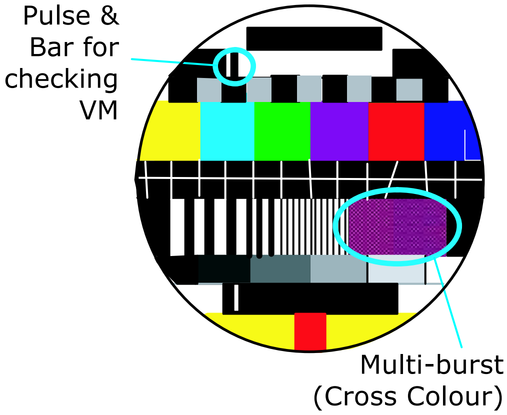
Adjust the horizontal picture position by changing RGB SHIFT.

2.2.5 COMBFILTER OPERATION
(100HZ/PROGRESSIVE SCAN MODELS)

Receive circle test pattern.

PICTURE »» MORE »» COMBFILTER by handset

Ensure the Comb Filter software option is ‘ON’ using handset, watching the multi-burst section of the test card, ensuring there is no ‘Cross Colour’ interference as shown.



2.2.6 VELOCITY MODULATION CHECK

Receive circle test pattern.

PICTURE »» MORE »» VM by handset

Check the bar width becomes sharper/narrow (see above) when VM is switched 'ON'.

2.2.7 SHORT CIRCUIT/DISTORTION CHECK OF MAIN AUDIO AMPLIFIER

With set in stereo mode, set spatialiser to OFF, receive a NICAM signal @ 400Hz Left & 1KHz Right, using the following channels:

Channel 26 for Export models
Channel 60 for UK models

Using a scope, adjust the volume control until a pure sine wave at the above frequencies is achieved at the left and right amplifier outputs. If a pure sine wave cannot be achieved, reject the set.

2.3 AUDIO SUB BOARDS

2.3.1 POWER AMPLIFIER BOARD FOR DOLBY DIGITAL SETS

All Models

Apply –17V (2 Amps) to E412 Pins 1+2.
Apply power supply ground to E412 Pins 3,4+5.
Apply +17V (2 Amps) to E412 Pins 6+7.

All Switchable Supplies Should Be High Until Turned Off

For CTV Models

Connect a switchable 5V Supply to E418 Pin 1.
Woofer Off
Connect a switchable 5V Supply to E418 Pin 2.
Rear Off
Connect a switchable 5V Supply to E418 Pin 3.
Centre Off

For 32" Models Connect Loads Capable Of Handling 30 Watts Across

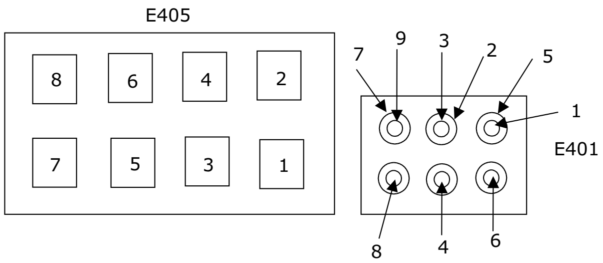
SW401 pressed in
E403 Pins 1+2 (8W).
E411 Pins 1+2 (4W).
E405 Pins 5+6 (8W).
E405 Pins 7+8 (8W).

For 36" Models Connect Loads Capable Of Handling 30 Watts Across

SW401 not fitted
E405 Pins 1+2 (4W).
E405 Pins 3+4 (8W).
E405 Pins 5+6 (8W).
E405 Pins 7+8 (8W).

For PTV Models

Connect a switchable 5V Supply to E409 Pin 13.
Vmute2
Connect a switchable 5V Supply to E409 Pin 14.
Mute
Connect a switchable 5V Supply to E409 Pin 15.
Woofer Off
Connect a switchable 5V Supply to E409 Pin 16.
Rear Off
Connect a switchable 5V Supply to E409 Pin 17.
Centre Off
SW401 pressed in
Connect loads capable of Handling 30 Watts across
E402 Pins 1+2 (8W).
E404 Pins 1+3 (8W).
E406 Pins 1+2 (8W).
E405 Pins 5+6 (8W).
E405 Pins 7+8 (8W).



Rear Right Channel

Apply 1KHz, 1Vrms signal to E414 Pin 3.
Check that an output of approximately 2Vrms is seen at E401 Pin 9 (Red).
Check that an output of approximately 9Vrms at E405 Pins 6.

Disconnect supply to E418 Pin 2/ E409 Pin 16 (Rear Off) both waveforms should disappear.

Supply 5V to E407 Pin 1/ E409 Pin 14 (Mute) both waveforms should disappear.
Supply 5V to E409 Pin 13 (Vmute2) both waveforms should disappear.

Rear Left Channel

Apply 1KHz, 1Vrms signal to E414 Pin 4.
Check that an output of approximately 2Vrms is seen at E401 Pin 8 (White).
Check that an output of approximately 9Vrms at E405 Pins 8.

Disconnect supply to E418 Pin 2/ E409 Pin 16 (Rear Off) both waveforms should disappear.

Supply 5V to E407 Pin 1/ E409 Pin 14 (Mute) both waveforms should disappear.
Supply 5V to E409 Pin 13 (Vmute2) both waveforms should disappear.

Front Right Channel

Apply 1KHz, 1Vrms signal to E414 Pin 7.
Check that an output of approximately 2Vrms is seen at E401 Pin 1 (Red).

Disconnect supply to E418 Pin 2/ E409 Pin 16 (Rear Off) both waveforms should disappear.

Supply 5V to E407 Pin 1/ E409 Pin 14 (Mute) waveform should disappear.
Supply 5V to E409 Pin 13 (Vmute2) waveform should disappear.

Front Left Channel

Apply 1KHz, 1Vrms signal to E414 Pin 8.
Check that an output of approximately 2Vrms is seen at E401 Pin 6 (White).

Supply 5V to E407 Pin 1/ E409 Pin 14 (Mute) waveform should disappear.
Supply 5V to E409 Pin 13 (Vmute2) waveform should disappear.

Centre Channel

Apply 1KHz, 1Vrms signal to E414 Pin 6.
Check that an output of approximately 2Vrms is seen at E401 Pin 4 (Green).
Check that an output of approximately 9Vrms at:
E404 Pin 1 – PTV.
E403 Pin 1 – 32'' CTV.
E405 Pin 4 – 36'' CTV.

Disconnect supply to E418 Pin 3/ E409 Pin 17 (Centre Off) both waveforms should disappear.

Supply 5V to E407 Pin 1/ E409 Pin 14 (Mute) both waveforms should disappear.
Supply 5V to E409 Pin 13 (Vmute2) both waveforms should disappear.

Woofer Channel

Apply 1KHz, 1Vrms signal to E414 Pin 5.
Check that an output of approximately 2Vrms is seen at E401 Pin 3 (Blue).
Check that an output of approximately 9Vrms at:
E402 Pin 1 &E406 Pin 1 – PTV.
E411 Pin 1 – 32'' CTV.
E405 Pin 1 – 36'' CTV.

Disconnect supply to E418 Pin 1/ E409 Pin 15 (Woofer Off) both waveforms should disappear.

Supply 5V to E407 Pin 1/ E409 Pin 14 (Mute) both waveforms should disappear.
Supply 5V to E409 Pin 13 (Vmute2) both waveforms should disappear.

2.3.2 DOLBY DIGITAL DECODER BOARD

DIGITAL AUDIO TEST

With the chassis in service mode, check that fault code 000E does not appear (indicates SRAM failure)

Using a DTS / Dolby Digital/MPEG compatible DVD Player with Optical and Coaxial digital audio out:

SETUP

With the chassis set to the correct AV input, the audio decode mode set to 'AUTO', the sound mode set to Dolby Pro Logic (or Dolby Digital if digital input already applied), the trims set to maximum, all speakers set to large, and the master volume at midway:-

Select track 72 on the Dolby Digital test DVD. Set the player for 'repeat play'.

Connect the coaxial output of the DVD player to E408 on the Audio Amplifier Board.

Check that the symbol Dolby D 3/2.1 appears. If it doesn't appear, press the recall/info button on the handset.

MUTING

Check with an oscilloscope that there are signals for all six channels on E401.

Using the remote control, mute the audio. Check that the signals at E401 disappear.

Un-mute the signal.

Next enter the digital audio setup menu and change the decode mode from ‘Auto’ to ‘Analogue’, to ‘Digital’ and then back to Auto. Make sure no ‘pop’ or ‘crack’ noises are heard on the speakers.

Access the speaker setup menu via the remote control and turn off all the amplifiers. Check pins 1,2, and 3 of PS08 of the decoder board go low. Any speakers connected should now be muted.

DOLBY DIGITAL TESTS

**Set the master volume control to maximum. Check that an undistorted continuous* sine wave can be seen at the following level on the channels below at the phono socket E401.

*The Audio will obviously show a transient as the track repeats. There should not be a glitch otherwise.

Signal	Level
L	2Vrms / 5.6Vpp @30Hz
R	2Vrms / 5.6Vpp @30Hz
C	2Vrms / 5.6Vpp @30Hz
LS	2Vrms / 5.6Vpp @30Hz
RS	2Vrms / 5.6Vpp @30Hz

At this point, it is normal that the woofer channel will show clipping. Turn the main volume down and check that you can achieve at least 3Vrms / 8.5 Vpp without clipping.

Remove the input to E408 and apply the optical input from the DVD player to I407.

Check the symbol Dolby D 3/2.1 appears (Press recall/info if it doesn’t) Repeat the test from **).

DTS

Select track 15 on the DTS test DVD. Set the player for ‘repeat play’.

Apply the coaxial output of the player to E408 on the audio amplifier board.

****Set the master volume control to maximum.

Check the OSD indicates DTS 3/2.1. If it doesn’t appear, press the recall/info button on the handset.

Check for an undistorted continuous*** sine wave can be seen at the following level on all channels at the phono socket E401.

Signal	Level
L	30Hz signal between 2Vrms and 2.1Vrms
R	30Hz signal between 2Vrms and 2.1Vrms
C	30Hz signal between 2Vrms and 2.1Vrms
LS	30Hz signal between 2Vrms and 2.1Vrms
RS	30Hz signal between 2Vrms and 2.1Vrms

***The Audio will obviously show a glitch as the track repeats. It should not glitch otherwise.

At this point, it is normal that the woofer channel will show clipping. Turn the main volume down and check that you can achieve at least 3Vrms / 8.5Vpp without clipping. Remove the input to E408 and apply the optical input from the DVD player to I407 and repeat the test from ****).

MPEG

Using an MPEG Multi-channel encoded disc, (such as the film ‘Jumanji’) apply the digital coaxial or optical output from the player to the amplifier board. Check the OSD displays MPEG Multi-ch. Check audio can be seen at all channels on E401.

ANALOGUE / PRO LOGIC MODE

Remove the digital source either from I407 or E408. Make sure the volume control is at Maximum.

Using a Pro logic encoder, apply a 2V 1KHz Lt Rt signal to the Audio inputs of the selected AV. Using a pro logic encoder, generate signals for each channel in turn (L, R, C and Surround) and make sure they appear undistorted at the correct outputs on E401. At the following levels:-

Signal	Level
L	1KHz signal between 2Vrms and 2.1Vrms
R	1KHz signal between 2Vrms and 2.1Vrms
C	1KHz signal between 2Vrms and 2.1Vrms
LS	1KHz signal between 1.41Vrms and 1.5Vrms
RS	1KHz signal between 1.4Vrms and 1.5Vrms

Put the master volume to mid way and un-mute the amplifiers via the speaker setup menu.

2.4 SHIPPING SPEC DATA SHEETS

SERVICE DATA SETTINGS - This is the data set in SERVICE mode for various models.													
	Model No.	Contrast	Brightness	Colour	Sharpness	Hue		Noise Reduction	Comb Filter	CTI	VM	White Point	Black Stretch
1*	C28WF523N – 311 50Hz	85%*	50%	50%	65%	50%		Auto	N/A	On	On	Normal	On
2*	C32WF523N – 311 50Hz	85%*	50%	50%	65%	50%		Auto	N/A	On	On	Normal	On
3*	C32WF720N - 311	85%*	50%	50%	65%	50%		Auto	On	On	On	Normal	Off
4*	C32WF810N - 311	85%*	50%	50%	65%	50%		Auto	On	On	On	Normal	Off
5*	D32WF815N - 311	85%*	50%	50%	65%	50%		Auto	On	On	On	Normal	Off
6	C36WF810N - 311	100%	50%	50%	65%	50%		Auto	On	On	On	Normal	Off
7	D36WF815TN - 311	100%	50%	50%	65%	50%		Auto	On	On	On	Normal	Off
8*	CL28WF720AN – 300	85%*	50%	50%	65%	50%		Auto	On	On	On	Normal	Off
9*	CL32WF720TAN - 300	85%*	50%	50%	65%	50%		Auto	On	On	On	Normal	Off
10*	CL32WF810AN – 300	85%*	50%	50%	65%	50%		Auto	On	On	On	Normal	Off
11	CL36WF810AN - 300	100%	50%	50%	65%	50%		Auto	On	On	On	Normal	Off
* Set contrast to 9 steps down from maximum.													

SERVICE DATA SETTINGS - This is the data set in SERVICE mode for various models.

	Model No.	Volume	Loudness	Balance	LFE		Mode	Graphic Equaliser		Sound Mode				3DS Mode
1	C28WF523N – 311 50Hz	10%	Off	50%	N/A		1	50%		Dolby Pro Logic				On
2	C32WF523N – 311 50Hz	10%	Off	50%	N/A		1	50%		Dolby Pro Logic				On
3	C32WF720N - 311	10%	Off	50%	N/A		1	50%		Stereo				N/A
4	C32WF810N - 311	10%	N/A	N/A	50%		1	50%		Dolby Digital				N/A
5	D32WF815N - 311	10%	N/A	N/A	50%		1	50%		Dolby Digital				N/A
6	C36WF810N - 311	10%	N/A	N/A	50%		1	50%		Dolby Digital				N/A
7	D36WF815TN - 311	10%	N/A	N/A	50%		1	50%		Dolby Digital				N/A
8	CL28WF720AN – 300	10%	Off	50%	N/A		1	50%		Stereo				N/A
9	CL32WF720TAN - 300	10%	Off	50%	N/A		1	50%		Stereo				N/A
10	CL32WF810AN – 300	10%	N/A	N/A	50%		1	50%		Dolby Digital				N/A
11	CL36WF810AN - 300	10%	N/A	N/A	50%		1	50%		Dolby Digital				N/A

SERVICE DATA SETTINGS - This is the data set in SERVICE mode for various models.

	Model No.	Sleep Timer	Default Zoom	Default 4:3	Auto Wide Detect		Display Mode	Scan Mode	Scan Speed		Language		
1	C28WF523N – 311 50Hz	Off	Panoramic	Panoramic	Off		N/A	N/A	N/A		English		
2	C32WF523N – 311 50Hz	Off	Panoramic	Panoramic	Off		N/A	N/A	N/A		English		
3	C32WF720N - 311	Off	Panoramic	Panoramic	Off		4	Channel	50%		English		
4	C32WF810N - 311	Off	Panoramic	Panoramic	Off		4	Channel	50%		English		
5	D32WF815N - 311	Off	Panoramic	Panoramic	Off		4	Channel	50%		English		
6	C36WF810N - 311	Off	Panoramic	Panoramic	Off		4	Channel	50%		English		
7	D36WF815TN - 311	Off	Panoramic	Panoramic	Off		4	Channel	50%		English		
8	CL28WF720AN – 300	Off	Panoramic	Panoramic	Off		4	Channel	50%		English		
9	CL32WF720TAN - 300	Off	Panoramic	Panoramic	Off		4	Channel	50%		English		
10	CL32WF810AN – 300	Off	Panoramic	Panoramic	Off		4	Channel	50%		English		
11	CL36WF810AN - 300	Off	Panoramic	Panoramic	Off		4	Channel	50%		English		

SERVICE DATA SETTINGS - This is the data set in SERVICE mode for various models.												
	Model No.	Surround Set-up	Pro Logic Seating Position		Sub Woofer Volume	Dolby Digital Seating Position	Centre Delay		Digital Input Source	Decode Mode	Listen Mode	
1	C28WF523N – 311 50Hz	100%	Mid		N/A	N/A	N/A		N/A	N/A	N/A	
2	C32WF523N – 311 50Hz	100%	Mid		N/A	N/A	N/A		N/A	N/A	N/A	
3	C32WF720N - 311	N/A	N/A		N/A	N/A	N/A		N/A	N/A	N/A	
4	C32WF810N - 311	100%	N/A		100%	Mid-Front	0mS		AV2	Auto	Maximum	
5	D32WF815N - 311	100%	N/A		100%	Mid-Front	0mS		AV2	Auto	Maximum	
6	C36WF810N - 311	100%	N/A		100%	Mid-Front	0mS		AV2	Auto	Maximum	
7	D36WF815TN - 311	100%	N/A		100%	Mid-Front	0mS		AV2	Auto	Maximum	
8	CL28WF720AN – 300	N/A	N/A		N/A	N/A	N/A		N/A	N/A	N/A	
9	CL32WF720TAN - 300	N/A	N/A		N/A	N/A	N/A		N/A	N/A	N/A	
10	CL32WF810AN – 300	100%	N/A		100%	Mid-Front	0mS		AV2	Auto	Maximum	
11	CL36WF810AN - 300	100%	N/A		100%	Mid-Front	0mS		AV2	Auto	Maximum	

SERVICE DATA SETTINGS - This is the data set in SERVICE mode for various models.													
	Model No.	Front L/R Speakers	Centre Speaker	Surround Speakers	Sub Woofer Speaker		Front Amp	Centre Amp	Rear Amp	Sub Woofer Amp		Internal Speakers	Centre Channel
1	C28WF523N – 311 50Hz	N/A	N/A	N/A	N/A		N/A	N/A	N/A	N/A		On	Phantom
2	C32WF523N – 311 50Hz	N/A	N/A	N/A	N/A		N/A	N/A	N/A	N/A		On	Phantom
3	C32WF720N - 311	N/A	N/A	N/A	N/A		N/A	N/A	N/A	N/A		On	N/A
4	C32WF810N - 311	Small	Small	Small	Large		On	On	On	On		N/A	N/A
5	D32WF815N - 311	Small	Small	Small	Large		On	On	On	On		N/A	N/A
6	C36WF810N - 311	Small	Small	Small	Large		On	On	On	On		N/A	N/A
7	D36WF815TN - 311	Small	Small	Small	Large		On	On	On	On		N/A	N/A
8	CL28WF720AN – 300	N/A	N/A	N/A	N/A		N/A	N/A	N/A	N/A		On	N/A
9	CL32WF720TAN - 300	N/A	N/A	N/A	N/A		N/A	N/A	N/A	N/A		On	N/A
10	CL32WF810AN – 300	Small	Small	Small	Large		On	On	On	On		N/A	N/A
11	CL36WF810AN - 300	Small	Small	Small	Large		On	On	On	On		N/A	N/A

SERVICE DATA SETTINGS - This is the data set in SERVICE mode for various models.

	Model No.	AV1 VCR Mode	AV1 SAV Mode	AV2 VCR Mode	AV2 Output Mode	AV3 VCR Mode		Def Std	Standards	VHF	AFC Offset	L’ Offset
1	C28WF523N – 311 50Hz	On	Auto	Off	RF	Off		I	I	Off	11	71
2	C32WF523N – 311 50Hz	On	Auto	Off	RF	Off		I	I	Off	11	71
3	C32WF720N - 311	On	Auto	Off	RF	Off		I	I	Off	11	71
4	C32WF810N - 311	On	Auto	Off	RF	Off		I	I	Off	11	71
5	D32WF815N - 311	On	Auto	Off	RF	Off		I	I	Off	11	71
6	C36WF810N - 311	On	Auto	Off	RF	Off		I	I	Off	11	71
7	D36WF815TN - 311	On	Auto	Off	RF	Off		I	I	Off	11	71
8	CL28WF720AN – 300	On	Auto	Off	RF	Off		BG	BG L I	On	11	71
9	CL32WF720TAN - 300	On	Auto	Off	RF	Off		BG	BG L I	On	11	71
10	CL32WF810AN – 300	On	Auto	Off	RF	Off		BG	BG L I	On	11	71
11	CL36WF810AN - 300	On	Auto	Off	RF	Off		BG	BG L I	On	11	71

SERVICE DATA SETTINGS - This is the data set in SERVICE mode for various models.

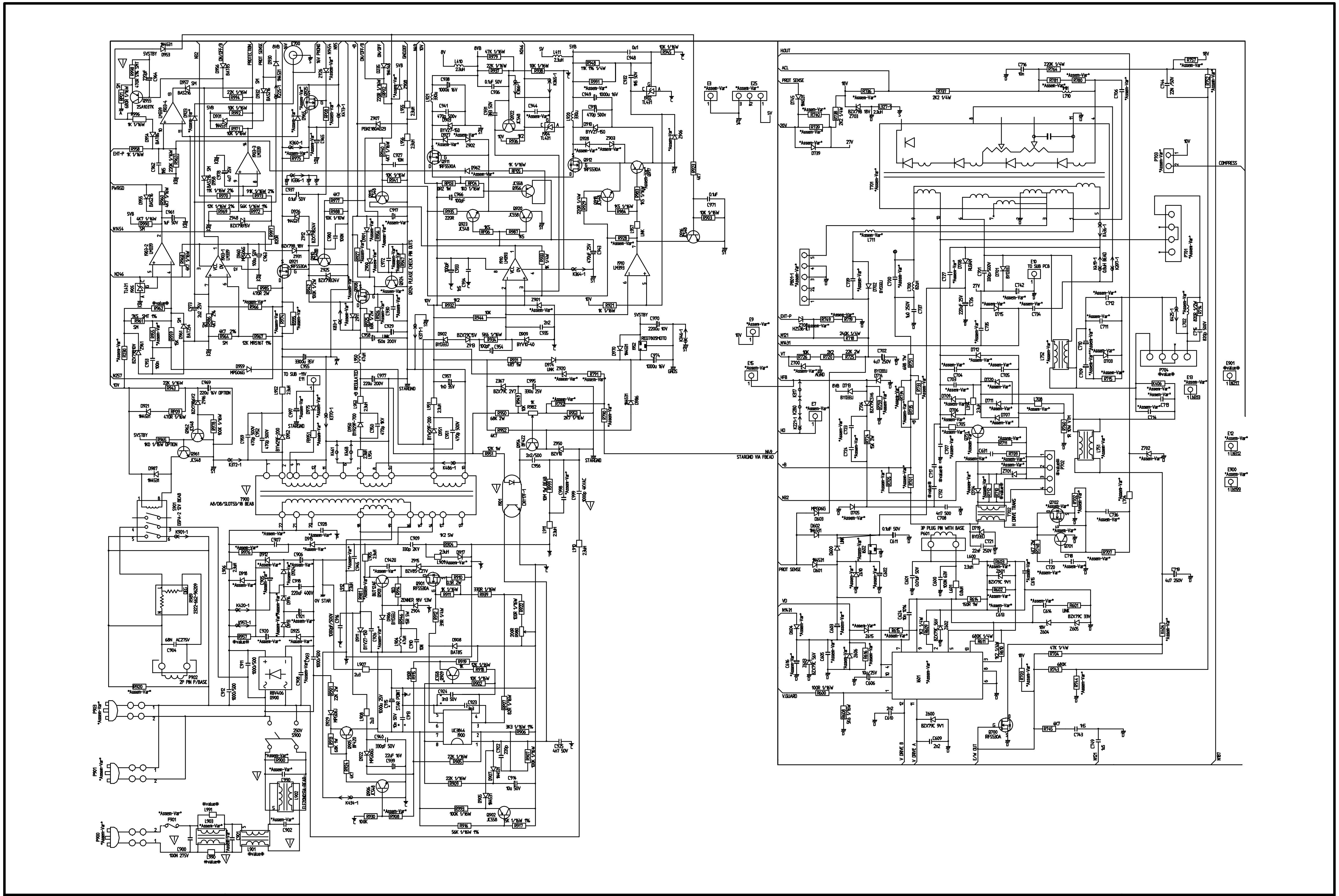
	Model No.	Text Shift		RGB Shift		R, G, B	Cool Offset	Warm Offset		Cathode Level	C Delay	Text Brightness	SECAM Offset
1	C28WF523N – 311 50Hz	31		35		31	4	4		86V	7	31	0
2	C32WF523N – 311 50Hz	31		35		31	4	4		86V	7	31	0
3	C32WF720N - 311	31		N/A		31	4	4		71V	3	31	0
4	C32WF810N - 311	31		N/A		31	4	4		71V	3	31	0
5	D32WF815N - 311	31		N/A		31	4	4		71V	3	31	0
6	C36WF810N - 311	31		N/A		31	4	4		77V	3	31	0
7	D36WF815TN - 311	31		N/A		31	4	4		77V	3	31	0
8	CL28WF720AN – 300	31		N/A		31	4	4		77V	3	31	0
9	CL32WF720TAN - 300	31		N/A		31	4	4		71V	3	31	0
10	CL32WF810AN – 300	31		N/A		31	4	4		71V	3	31	0
11	CL36WF810AN - 300	31		N/A		31	4	4		77V	3	31	0

SERVICE DATA SETTINGS - This is the data set in SERVICE mode for various models.

	Model No.	Current Text Mode		Text Modes	LG Tube Type	M Gating	Options Byte	Positive Sync	OSD Position		100Hz/ Progressive Scan		Digital/ Analogue Mode
1	C28WF523N – 311 50Hz	Single		SDS	Off	Off	03	Off	27		N/A		Analogue
2	C32WF523N – 311 50Hz	Single		SDS	On	Off	03	Off	27		N/A		Analogue
3	C32WF720N - 311	Single		SDS	On	Off	03	On	27		Progressive		Analogue
4	C32WF810N - 311	Single		SDS	On	Off	07	On	27		Progressive		Analogue
5	D32WF815N - 311	Single		SDS	On	Off	07	On	27		Progressive		Digital
6	C36WF810N - 311	Single		SDS	Off	Off	07	On	27		Progressive		Analogue
7	D36WF815TN - 311	Single		SDS	Off	Off	07	On	27		Progressive		Digital
8	CL28WF720AN – 300	Single		SDS+T	Off	Off	0B	On	27		Progressive		Analogue
9	CL32WF720TAN - 300	Single		SDS+T	On	Off	0B	On	27		Progressive		Analogue
10	CL32WF810AN – 300	Single		SDS+T	On	Off	0F	On	27		Progressive		Analogue
11	CL36WF810AN - 300	Single		SDS+T	Off	Off	0F	On	27		Progressive		Analogue

SERVICE DATA SETTINGS - This is the data set in SERVICE mode for various models.

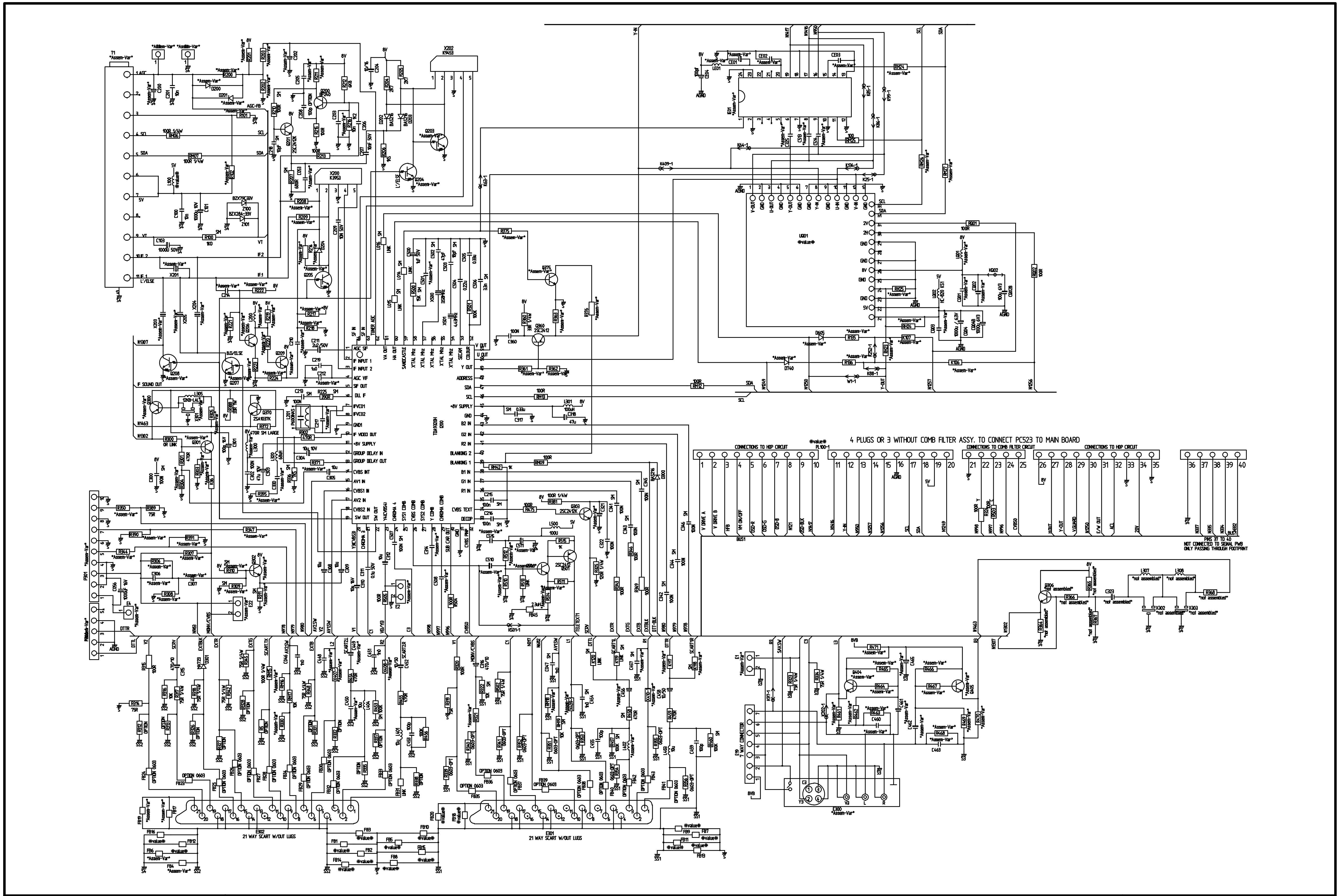
	Model No.	Hotel Mode	No Standby	Prog.	Max. Volume	DTT Prog.						
1	C28WF523N – 311 50Hz	Off	On	1	50%	1						
2	C32WF523N – 311 50Hz	Off	On	1	50%	1						
3	C32WF720N - 311	Off	On	1	50%	1						
4	C32WF810N - 311	Off	On	1	50%	1						
5	D32WF815N - 311	Off	On	1	50%	1						
6	C36WF810N - 311	Off	On	1	50%	1						
7	D36WF815TN - 311	Off	On	1	50%	1						
8	CL28WF720AN – 300	Off	On	1	50%	1						
9	CL32WF720TAN - 300	Off	On	1	50%	1						
10	CL32WF810AN – 300	Off	On	1	50%	1						
11	CL36WF810AN - 300	Off	On	1	50%	1						


HOUT
ACL
PROT SENSE
COMPRESS
PWRSID
ENT-P
N1454
N246
N257
5VSTBY
TO SUB -11V
E11
STARGND
STARGND VIA FBEAD
T900
A8/D8/SLOT53/18 BEAB
T701
TO SUB PCB
E10
E9
E15
E7
E13
E901
E12
E900
P701
P702
P704
P601
3P PLUG PIN WITH BASE
H DRIVE TRANS
T702
IC601
IC900
UC3844
IC910
LM393
RBV406
D900
CRT/FF-1
P901
P902
2P PIN P/BASE
P903
P900
S900
250V
F901
L901
L903
C900
100N 275V
RB40C6
IRF5530A
IRFS530A
IRF5530A
TL431
REG7809HDT0
Q912
Q911
Q700
Q701
Q702
0V STAR
STAR POINT
ZENNER 18V 1.3W
PLEASE CHECK PIN OUTS
V DRIVE B
V DRIVE A
E/W OUT
N121
NK9
VD
VT
HFB
HD
N932
N1431
V.GUARD
+B
Assem-Var

No 00025

MAIN BOARD SCHEMATIC (1 of 3)

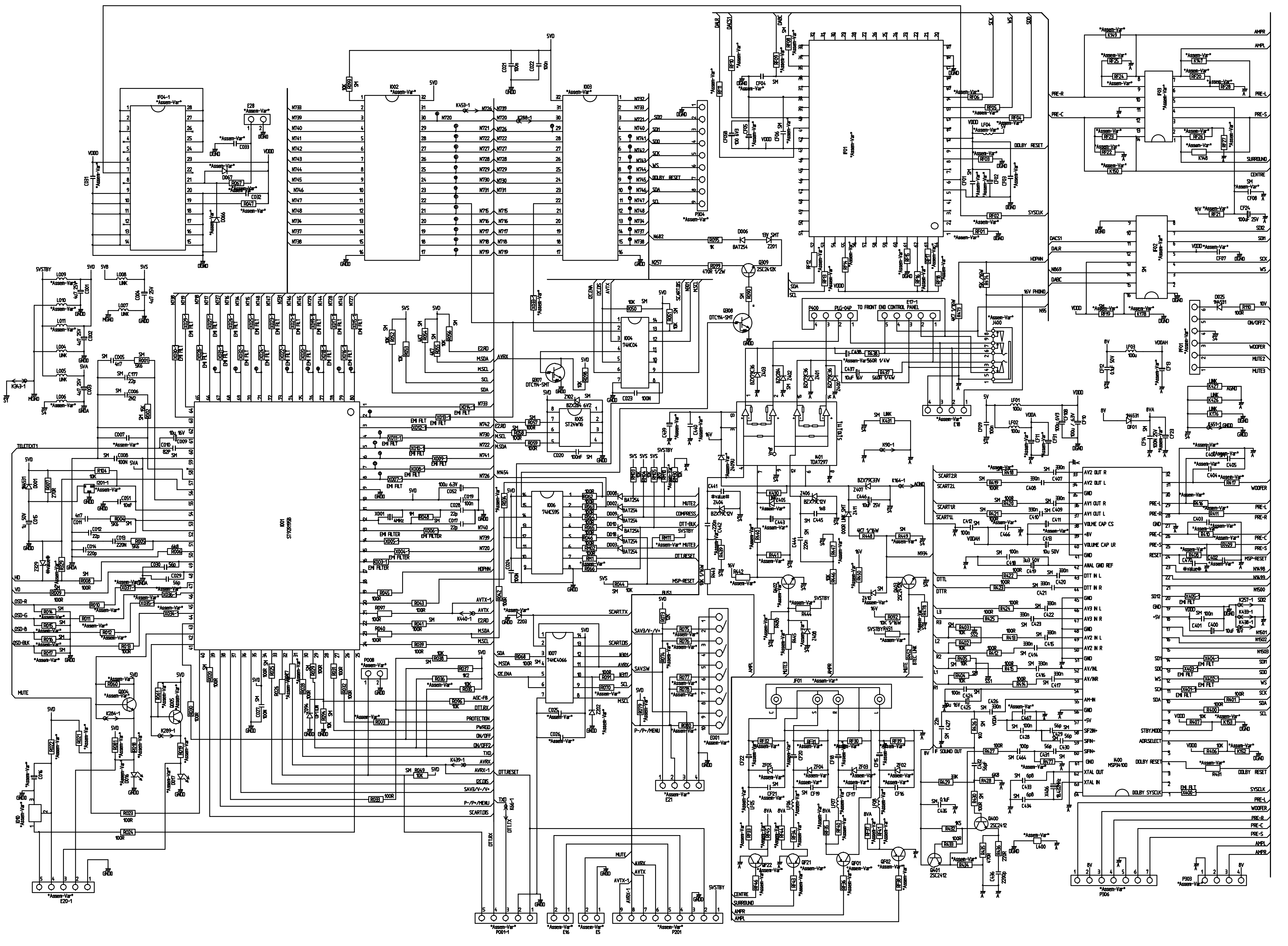
HITACHI


4 PLUGS OR 3 WITHOUT COMB FILTER ASSY. TO CONNECT PC523 TO MAIN BOARD
CONNECTIONS TO HDP CIRCUIT
CONNECTIONS TO COMB FILTER CIRCUIT
CONNECTIONS TO HDP CIRCUIT
PINS 37 TO 40
NOT CONNECTED TO SIGNAL PWB
ONLY PASSING THROUGH FOOTPRINT
TDA9320H
U001
X202
K9453
X200
K3953
E302
21 WAY SCART W/OUT LUGS
E301
21 WAY SCART W/OUT LUGS
E9
7 WAY CONNECTOR
P301
T1

No 00025

MAIN BOARD SCHEMATIC (2 of 3)

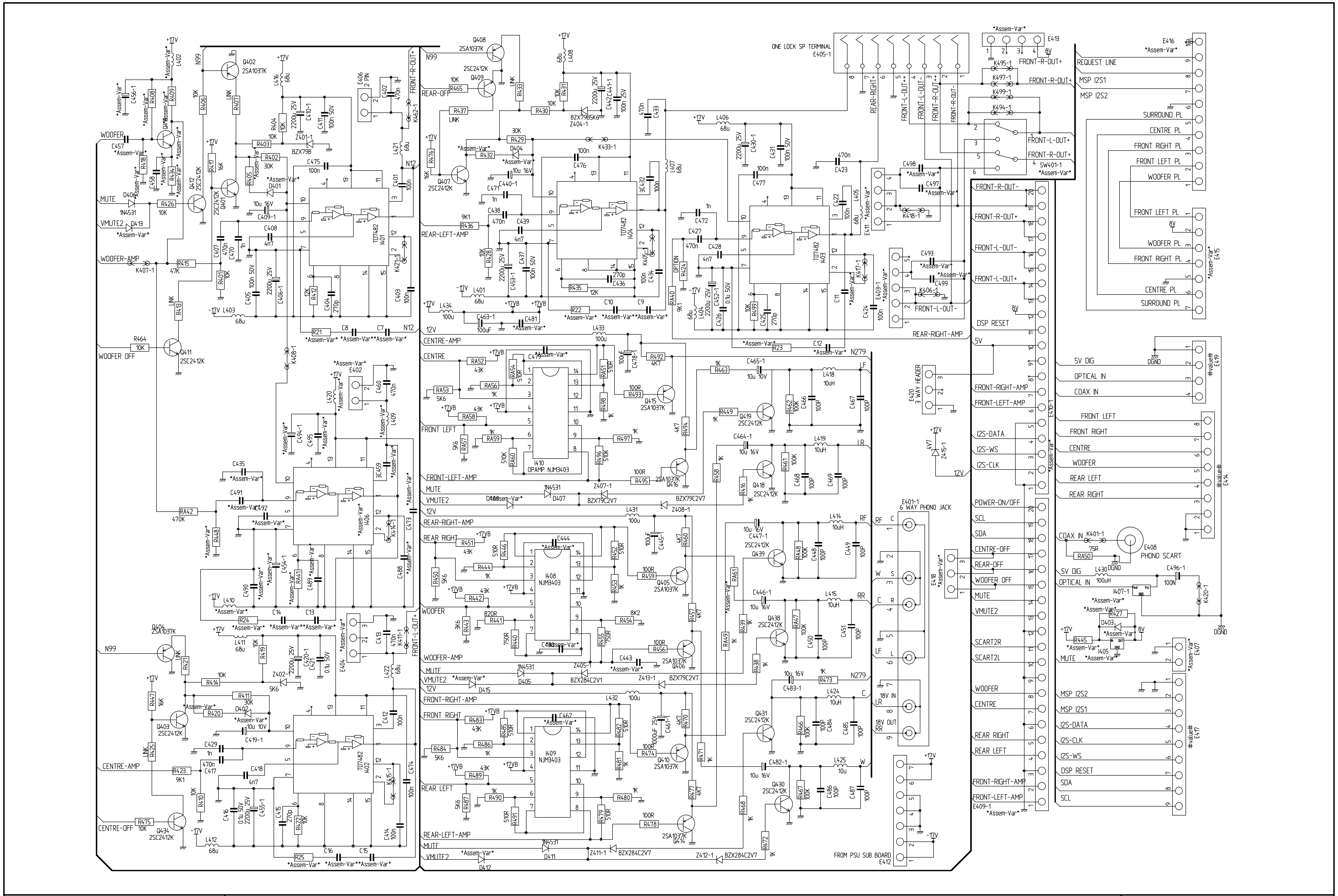
HITACHI


I001
ST92R195B
I002
I003
I004
74HC04
I005
ST24W16
I006
74HC595
I007
74HC4066
I401
TDA7297
I400
MSP34100
IF01
IF02
IF03
IF04-1
P304
P400
PLG-04P
TO FRONT END CONTROL PANEL
E17-1
J400
E18
E20-1
E21
E001
JF01
P001-1
E16
E5
P201
P306
P303
P009
E28
TELETEXT1
MUTE
VDDD
SVD
SVSTBY
AMPR
AMPL
PRE-R
PRE-L
PRE-C
PRE-S
SURROUND
CENTRE
WOOFER
MUTE2
MUTE3
ON/OFF2
DOLBY RESET
SYSCLK
HDPHN
DACS1
DALR
DABC
SDA
SCL
AVTX
AVRX
MSDA
MSCL
DTT.RESET
DTT.TX
DTT.RX
PROTECTION
PWRGD
ON/OFF
SCARTDS
Assem-Var

No 00025

MAIN BOARD SCHEMATIC (3 of 3)

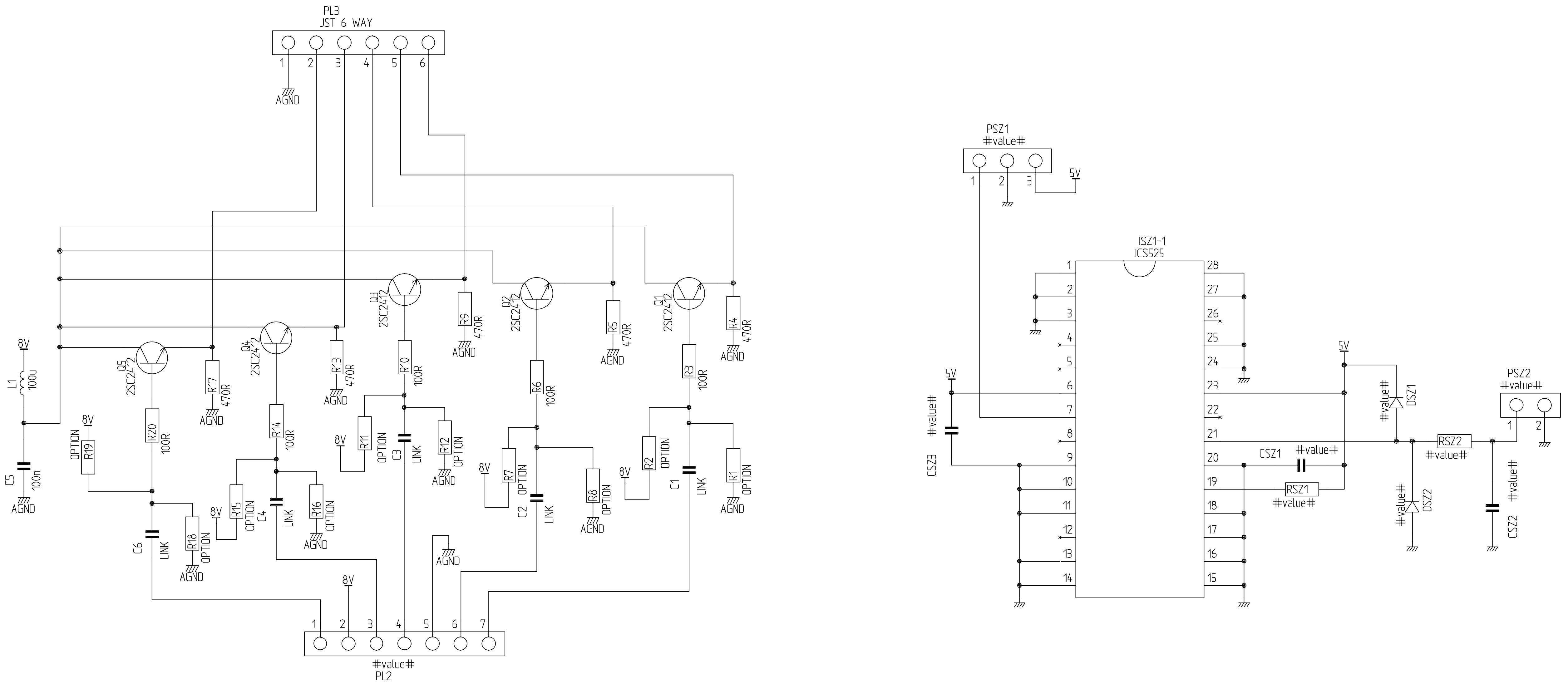
HITACHI


ONE LOCK SP TERMINAL
E405-1
REAR-RIGHT-
FRONT-L-OUT+
FRONT-L-OUT-
FRONT-R-OUT+
FRONT-R-OUT-
Assem-Var
E413
FRONT-R-OUT+
E416
REQUEST LINE
MSP I2S1
MSP I2S2
SURROUND PL
CENTRE PL
FRONT RIGHT PL
FRONT LEFT PL
WOOFER PL
SW401-1
E415
WOOFER
MUTE
VMUTE2
WOOFER-AMP
WOOFER OFF
N99
N12
N279
Q402 2SA1037K
Q408 2SA1037K
Q409 2SC2412K
Q407 2SC2412K
Q401 2SC2412K
Q412 2SC2412K
Q411 2SC2412K
TDA7482 I401
TDA7482 I404
TDA7482 I403
TDA7482 I406
TDA7482 I402
REAR-OFF
REAR-LEFT-AMP
REAR-RIGHT-AMP
FRONT-R-OUT-
FRONT-L-OUT-
E411
E403-1
DSP RESET
5V
12V
CENTRE-AMP
CENTRE
FRONT LEFT
FRONT-LEFT-AMP
FRONT-RIGHT-AMP
FRONT RIGHT
REAR RIGHT
REAR LEFT
I410 OPAMP NJM3403
I408 NJM3403
I409 NJM3403
Q415 2SA1037K
Q416 2SA1037K
Q419 2SC2412K
Q418 2SC2412K
Q405 2SA1037K
Q406 2SA1037K
Q410 2SA1037K
Q414 2SA1037K
Q439 2SC2412K
Q438 2SC2412K
Q431 2SC2412K
Q430 2SC2412K
Q404 2SA1037K
Q403 2SC2412K
Q434 2SC2412K
CENTRE-OFF
E401-1 6 WAY PHONO JACK
E420 3 WAY HEADER
E418
5V DIG
OPTICAL IN
COAX IN
DGND
E419
E414
POWER-ON/OFF
SCL
SDA
I2S-DATA
I2S-WS
I2S-CLK
SCART2R
SCART2L
E410-1
E409-1
E408 PHONO SCART
E407
E417
I405
I407-1
FROM PSU SUB BOARD
E412
18V IN
18V OUT
LF
LR
RF
RR
C
W
+17V
-17V
+17VB
BZX79C2V7
BZX284C2V1
BZX284C2V7
1N4531

No 00025

AUDIO AMP SCHEMATIC (1 OF 2)

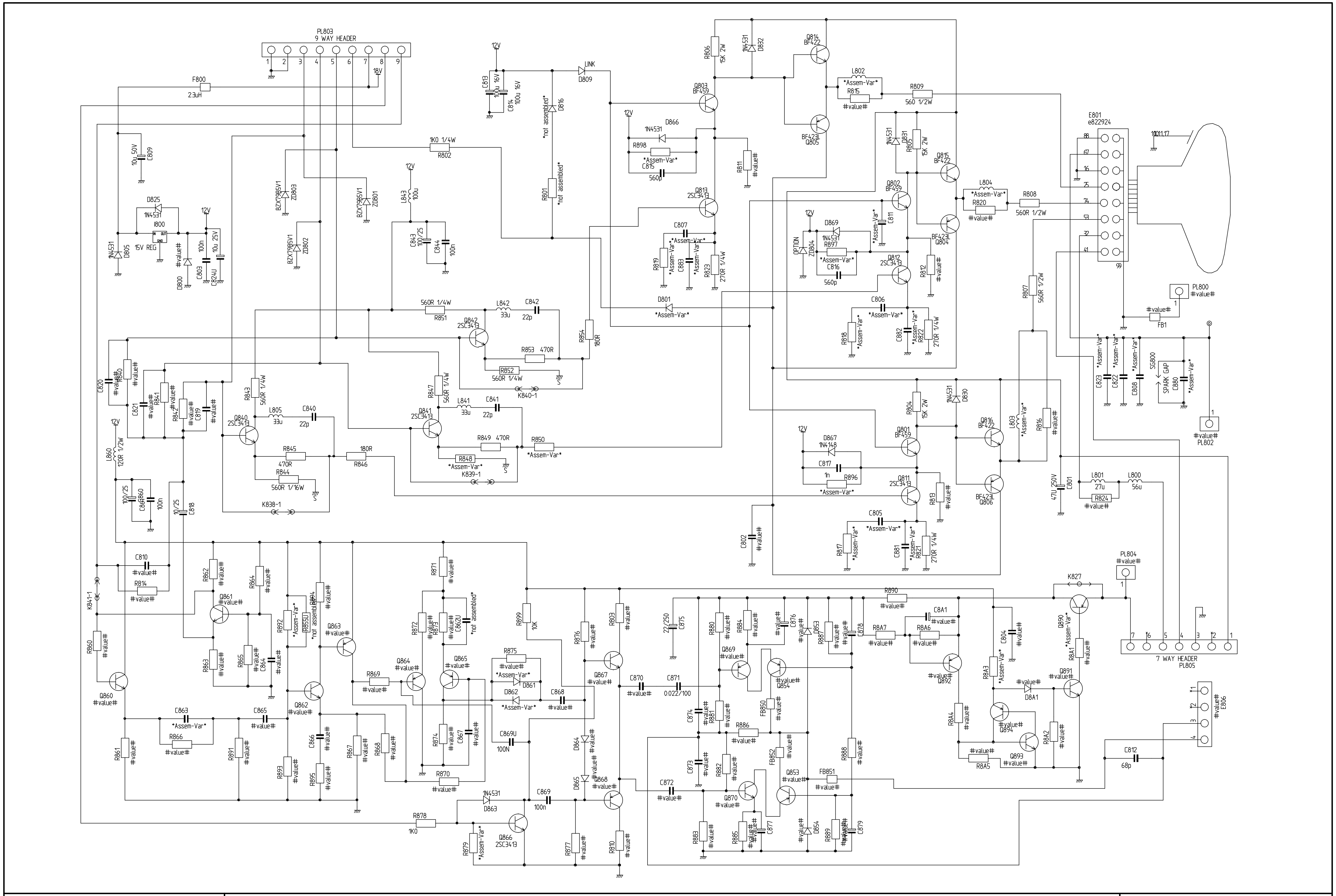
HITACHI


PL3
JST 6 WAY
1
2
3
4
5
6
AGND
Q1
2SC2412
Q2
2SC2412
Q3
2SC2412
Q4
2SC2412
Q5
2SC2412
R1
OPTION
R2
OPTION
R3
100R
R4
470R
R5
470R
R6
100R
R7
OPTION
R8
OPTION
R9
470R
R10
100R
R11
OPTION
R12
OPTION
R13
470R
R14
100R
R15
OPTION
R16
OPTION
R17
470R
R18
OPTION
R19
OPTION
R20
100R
C1
LINK
C2
LINK
C3
LINK
C4
LINK
C5
100n
C6
LINK
L1
100u
8V
PL2
#value#
7
PSZ1
#value#
5V
ISZ1-1
ICS525
CSZ1
CSZ2
CSZ3
RSZ1
RSZ2
DSZ1
DSZ2
PSZ2

No 00025

AUDIO AMP SCHEMATIC (2 OF 2)

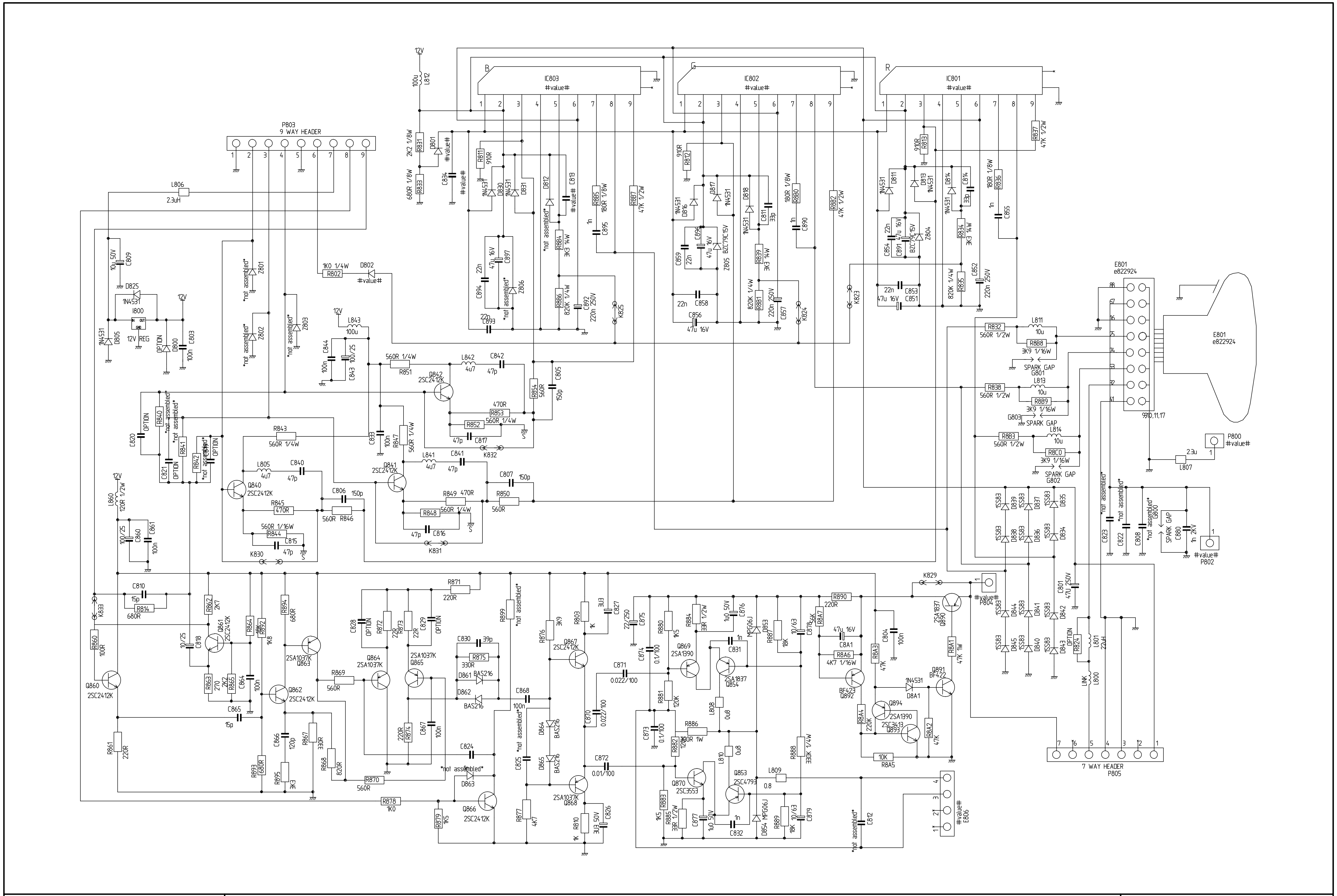
HITACHI


PL803
9 WAY HEADER
F800
23uH
18V
12V
C813
C814
100u 16V
D809
LINK
D816
not assembled
R801
1K0 1/4W
R802
C809
10u 50V
D825
1N4531
I800
15V REG
D805
D800
C803
100n
C824U
10u 25V
ZD803
ZD801
ZD802
BZX79C5V1
L843
100u
C843
100/25
C844
100n
R806
15K 2W
D832
Q814
BF422
Q803
BF459
L802
Assem-Var
R815
#value#
R809
560 1/2W
Q805
BF423
D866
1N4531
R898
C815
560p
R811
Q813
2SC3413
C807
R819
C883
R823
270R 1/4W
D801
E801
e822924
Q802
BF459
D831
R805
15K 2W
Q815
BF422
L804
R820
R808
560R 1/2W
Q804
BF423
D869
R897
C816
560p
ZD804
OPTION
C811
Q812
2SC3413
R812
C806
R818
C882
R822
R807
560R 1/2W
PL800
FB1
C823
C822
C808
SG800
SPARK GAP
C880
PL802
R851
560R 1/4W
L842
33u
C842
22p
Q842
2SC3413
R853
470R
R852
560R 1/4W
K840-1
R854
180R
C820
R840
C821
R841
R842
C819
R843
560R 1/4W
Q840
2SC3413
L805
33u
C840
22p
R847
560R 1/4W
Q841
2SC3413
L841
33u
C841
22p
R849
470R
R850
R848
K839-1
R845
470R
R846
180R
R844
560R 1/16W
K838-1
L860
120R 1/2W
C860
100/25
100n
C818
10/25
R804
15K 2W
D830
Q801
BF459
Q816
BF422
L803
R816
D867
1N4148
C817
1n
R896
Q811
2SC3413
R813
Q806
BF423
C801
47U 250V
L801
27u
L800
56u
R824
C805
C802
R817
C881
R821
270R 1/4W
C810
R814
K841-1
R862
R864
Q861
R863
R865
C864
R892
R855U
R894
not assembled
Q863
R860
Q860
C863
R866
C865
Q862
R861
R891
R893
C866
R895
R867
R868
R871
R872
R873
C862U
R869
Q864
Q865
R874
C867
R870
R899
10K
R875
D861
D862
C868
C869U
100N
R876
R803
Q867
C870
C871
0.022/100
C875
22/250
D864
D865
Q868
C869
100n
1N4531
D863
Q866
2SC3413
R878
1K0
R879
R877
R810
C872
R880
R884
C876
D853
R887
C878
Q869
Q854
C874
R881
FB850
R886
C873
R882
FB852
Q853
Q870
R883
R885
C877
D854
R889
C879
FB851
R888
R890
C8A1
R8A7
R8A6
Q892
C804
R8A3
D8A1
Q891
R8A4
Q894
Q893
R8A2
R8A5
R8A1
Q890
K827
PL804
7 WAY HEADER
PL805
E806
C812
68p
#value#
Assem-Var

No 00025

CRT SCHEMATIC

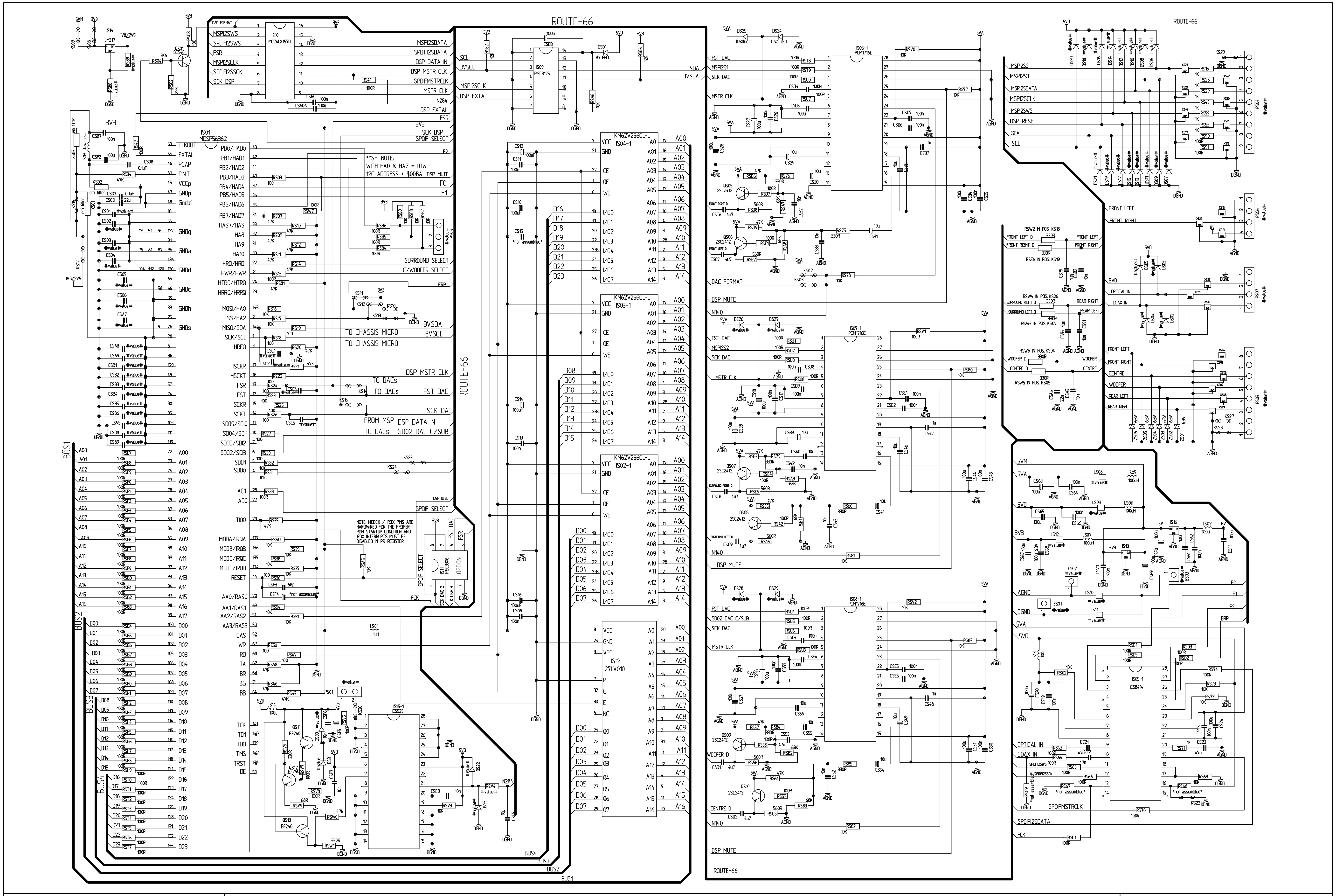
HITACHI


12V
L812
100u
IC803
#value#
B
IC802
G
IC801
R
1 2 3 4 5 6 7 8 9
P803
9 WAY HEADER
L806
2.3uH
C809
10u 50V
D825
1N4531
I800
12V REG
D805
D800
C803
OPTION
Z801
Z802
Z803
not assembled
R802
1K0 1/4W
D802
L843
100u
C844
C843
100/25
R851
560R 1/4W
L842
4u7
C842
47p
Q842
2SC2412K
R854
560R
C805
150p
R853
470R
R852
560R 1/4W
C817
K832
R843
560R 1/4W
C833
100n
R847
Q841
2SC2412K
L841
C841
C807
150p
R849
470R
R850
560R
R848
560R 1/4W
C816
K831
Q840
2SC2412K
L805
C840
C806
150p
R845
470R
R846
560R
R844
560R 1/16W
C815
K830
R840
R841
R842
C820
C821
L860
120R 1/2W
C860
100/25
C861
C810
15p
R814
680R
K833
R860
100R
Q860
2SC2412K
R861
220R
R862
2K7
Q861
2SC2412K
C818
10/25
R863
R865
R864
C864
R892
1K8
Q862
2SC2412K
C865
15p
C866
120p
R867
330R
R893
680R
R895
3K3
R894
680R
Q863
2SA1037K
R869
560R
R868
820R
R870
560R
R878
1K0
R879
1K5
C828
R872
R873
22R
C829
OPTION
Q864
2SA1037K
Q865
2SA1037K
R874
220R
C867
100n
R871
220R
C830
39p
R875
330R
D861
BAS216
D862
C824
D863
Q866
2SC2412K
R899
C868
100n
C825
R877
4K7
D864
D865
BAS216
R876
3K9
R803
1K
C827
3E3
Q867
2SC2412K
C870
0.022/100
C871
0.022/100
C872
0.01/100
Q868
2SA1037K
R810
1K
C826
3u3 50V
C875
22/250
C874
0.1/100
R880
1K5
R884
33R 1/2W
C876
1u0 50V
Q869
2SA1390
C831
1n
Q854
2SA1837
D853
MPG06J
R887
18K
C878
10/63
R881
120K
C873
0.1/100
R886
330R 1W
R882
120
L808
0u8
L810
0u8
Q870
2SC3553
Q853
2SC4793
R883
1K5
R885
33R 1/2W
C877
1u0 50V
C832
1n
D854
MPG06J
R889
18K
C879
10/63
R888
330K 1/4W
L809
0.8
C812
E806
R890
220R
R8A7
56K
C8A1
47u 16V
R8A6
4K7 1/16W
Q892
BF423
C804
100n
R8A3
47K
Q890
2SA1837
R8A1
47K 1W
Q891
BF422
D8A1
1N4531
Q894
2SA1390
Q893
2SC3413
R8A4
220K
R8A2
47K
R8A5
10K
K829
P804
P805
7 WAY HEADER
1 2 3 4 5 6 7
L801
22uH
LINK
L800
R824
OPTION
E801
e822924
9,10,11,17
R832
560R 1/2W
L811
10u
R888
3K9 1/16W
SPARK GAP
G801
R838
560R 1/2W
L813
R889
G803
R883
L814
R8C0
G802
P800
L807
2.3u
D835
D836
D837
D838
D839
D834
D840
D841
D842
D843
D844
D845
1SS83
C823
C822
C808
G800
C880
1n 2KV
P802
C801
47u 250V
R831
2K2 1/8W
R833
680R 1/8W
D801
C834
R811
910R
D830
D831
1N4531
D812
C813
R885
180R 1/8W
R887
47K 1/2W
C895
1n
R884
3K3 1/4W
R886
820K 1/4W
C892
220n 250V
C894
22n
C897
47u 16V
Z806
C893
K825
R812
910R
D816
D817
D818
C811
33p
R880
180R 1/8W
C890
R882
47K 1/2W
C859
C896
Z805
BZC79C15V
R839
3K3 1/4W
R881
820K 1/4W
C857
220n 250V
C858
C856
47u 16V
K824
K823
R813
910R
D811
D813
D814
C814
33p
R836
180R 1/8W
C855
R837
47K 1/2W
C854
C891
Z804
R834
3K3 1/4W
R835
820K 1/4W
C852
220n 250V
C853
C851

No 00025

CRT524 SCHEMATIC

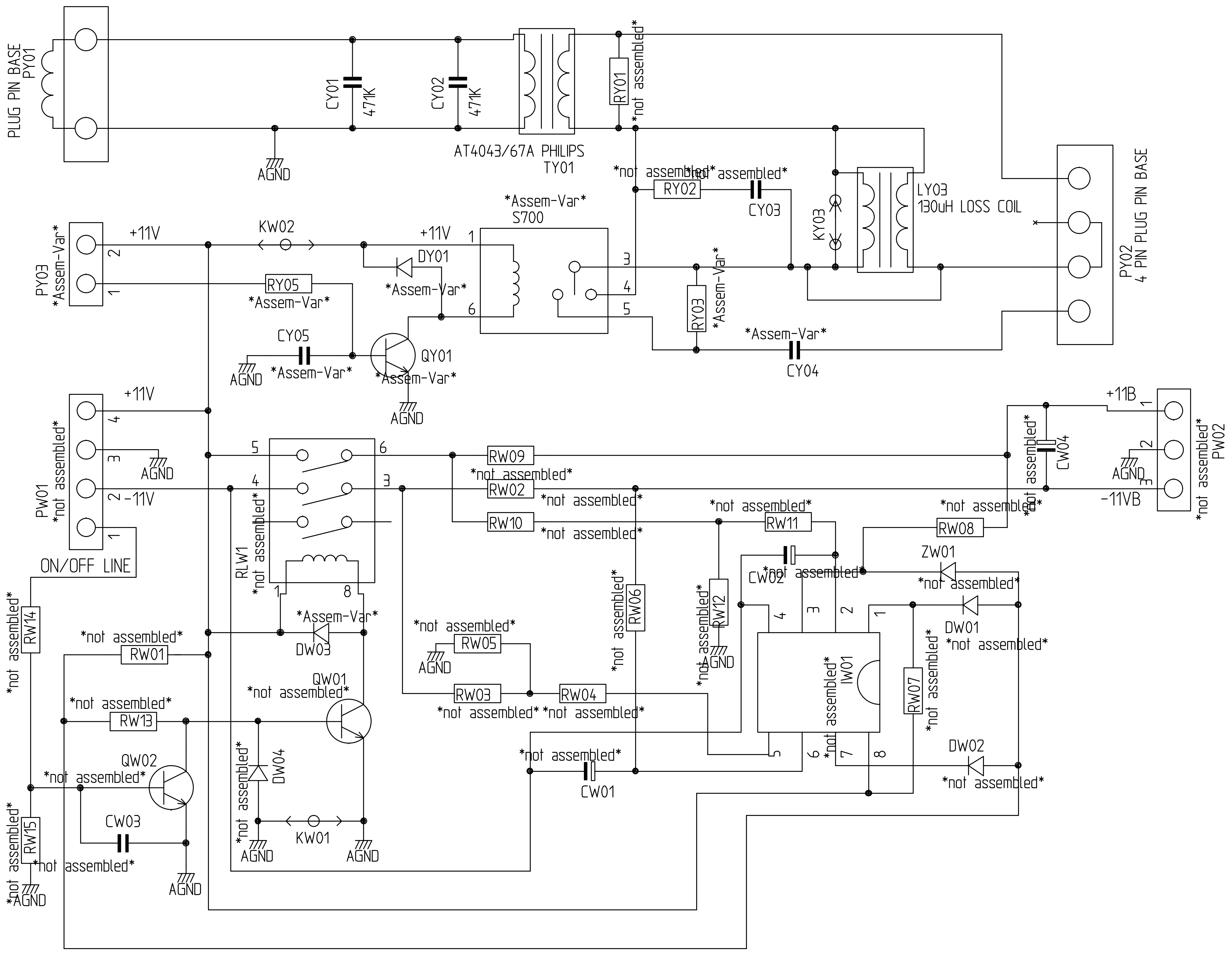
HITACHI


ROUTE-66
IS10 MC74LX1570
IS09 P6C3125
IS01 MDSP56362
KM62V256CL-L IS04-1
KM62V256CL-L IS03-1
KM62V256CL-L IS02-1
IS12 27LV010
IS15-1 IC5525
IS11 P6C1306
IS06-1 PCM1716E
IS07-1 PCM1716E
IS08-1 PCM1716E
IS05-1 CS8414
IS14 LM317
**SHI NOTE:
WITH HA0 & HA2 = LOW
12C ADDRESS = $00BA
NOTE: MODEX / IRQX PINS ARE HARDWIRED FOR THE PROPER ROM STARTUP CONDITION AND IRQX INTERRUPTS MUST BE DISABLED IN IPR REGISTER.
TO CHASSIS MICRO
TO DACs
FROM MSP
DSP DATA IN
DSP MSTR CLK
FST DAC
SCK DAC
SD02 DAC C/SUB
SURROUND SELECT
C/WOOFER SELECT
SPDIF SELECT
DSP EXTAL
DSP RESET
DSP MUTE
DAC FORMAT
MSPI2SWS
SPDIFI2SWS
MSPI2SCLK
SPDIFI2SSCK
MSPI2SDATA
SPDIFI2SDATA
SPDIFMSTRCLK
MSTR CLK
SCK DSP
FSR
3VSDA
3VSCL
SDA
SCL
FRONT LEFT
FRONT RIGHT
CENTRE
WOOFER
REAR LEFT
REAR RIGHT
OPTICAL IN
COAX IN
BUS1
BUS2
BUS3
BUS4
5VA
5VD
3V3
AGND
DGND

No 00025

DIGITAL DECODER

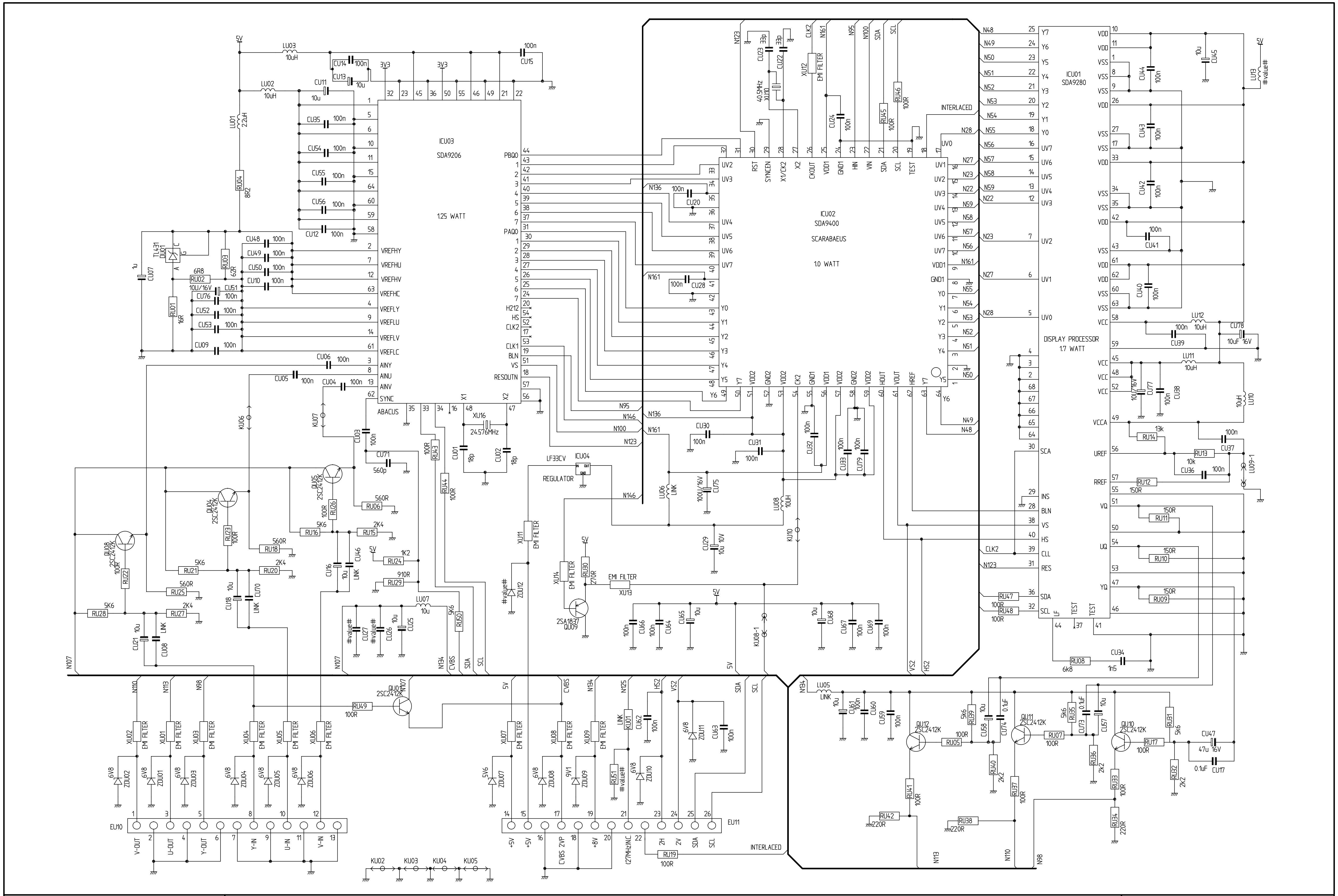
HITACHI


PLUG PIN BASE
PY01
CY01
471K
CY02
471K
AGND
AT4043/67A PHILIPS
TY01
RY01
not assembled
not assembled
RY02
not assembled
CY03
KY03
LY03
130uH LOSS COIL
PY02
4 PIN PLUG PIN BASE
PY03
Assem-Var
+11V
KW02
+11V
Assem-Var
S700
DY01
Assem-Var
RY05
Assem-Var
RY03
Assem-Var
CY05
Assem-Var
QY01
Assem-Var
AGND
Assem-Var
CY04
PW01
not assembled
+11V
AGND
-11V
ON/OFF LINE
RLW1
not assembled
RW09
not assembled
RW02
not assembled
RW10
not assembled
RW11
not assembled
RW08
not assembled
CW04
not assembled
+11B
AGND
-11VB
PW02
not assembled
CW02
not assembled
ZW01
not assembled
DW01
not assembled
IW01
not assembled
RW07
not assembled
DW02
not assembled
RW06
not assembled
RW12
not assembled
AGND
RW14
not assembled
RW01
not assembled
Assem-Var
DW03
QW01
not assembled
RW05
not assembled
AGND
RW03
not assembled
RW04
not assembled
RW13
not assembled
QW02
not assembled
DW04
not assembled
CW01
not assembled
CW03
not assembled
RW15
not assembled
AGND
KW01
AGND
AGND
AGND

No 00025

FOCUS ASSY SCHEMATIC

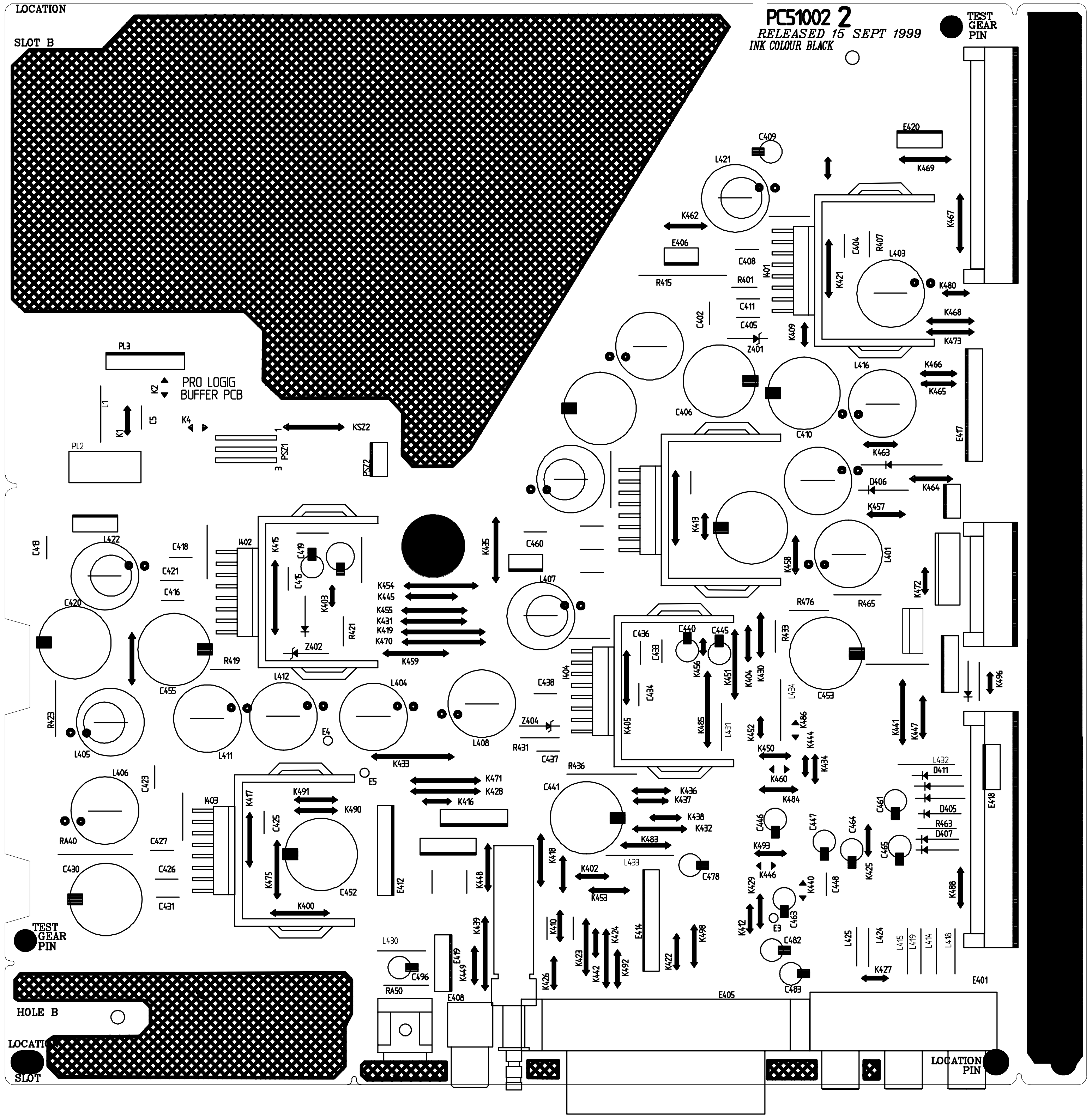
HITACHI


ICU03
SDA9206
1.25 WATT
ABACUS
ICU02
SDA9400
SCARABAEUS
1.0 WATT
ICU01
SDA9280
DISPLAY PROCESSOR
1.7 WATT
ICU04
LF33CV
REGULATOR
XU16
24.576MHz
40.5MHz
XU10
TL431
DU01
QU04
2SC2412K
QU05
2SC2412K
QU08
2SC2412K
QU07
2SC2412K
QU09
2SA1837
QU10
2SC2412K
QU11
2SC2412K
QU12
2SC2412K
EMI FILTER
EU10
EU11
V-OUT
U-OUT
Y-OUT
Y-IN
U-IN
V-IN
+5V
CVBS 2VP
+8V
(27MHz)NC
2H
2V
SDA
SCL
INTERLACED
KU02
KU03
KU04
KU05
5V
3V3
N107
N110
N113
N98
N134
N146
N123
N136
N161
N100
N95
CLK2
VS2
HS2

No 00025

FEATURE BOX SCHEMATIC

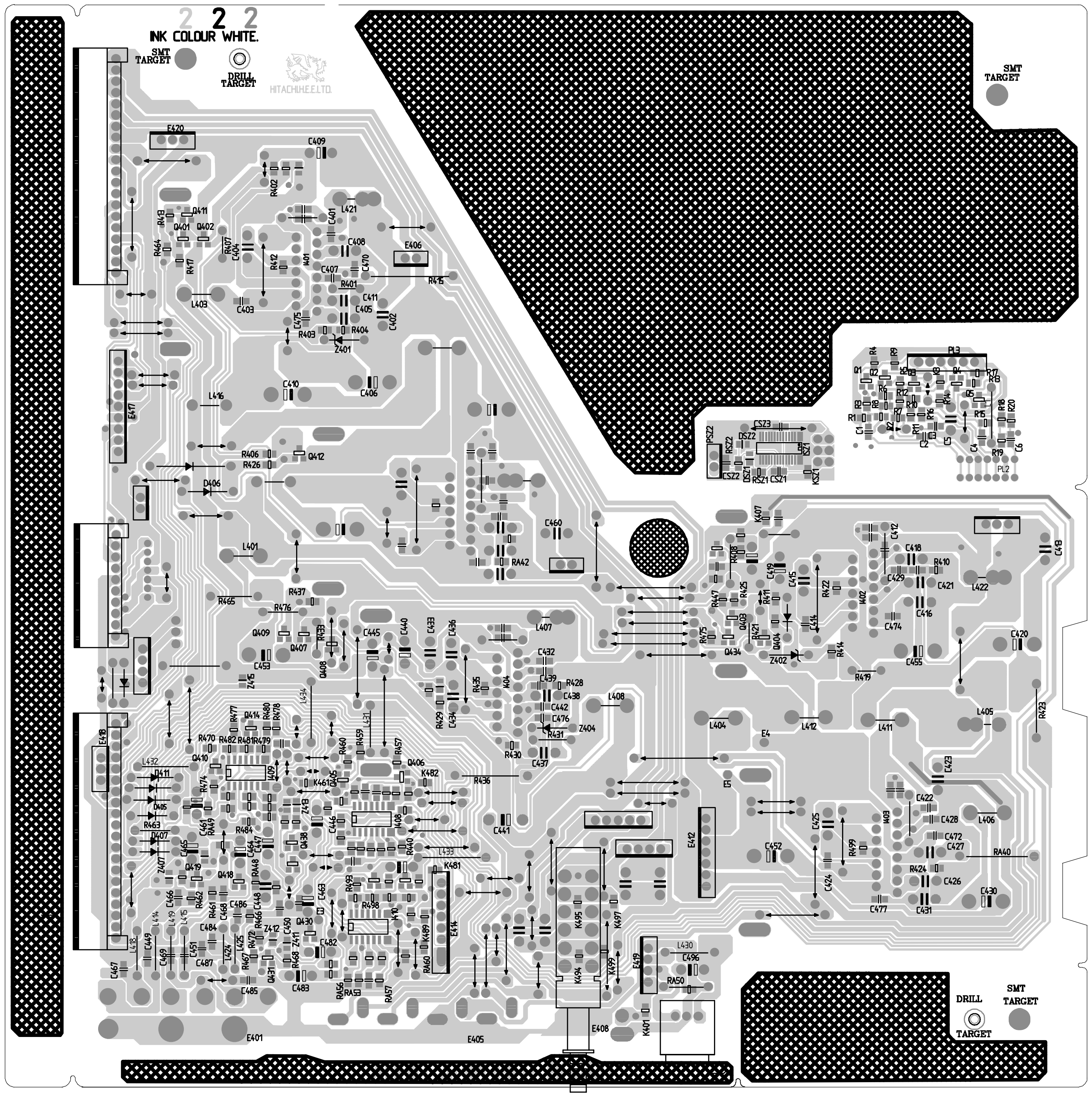
HITACHI


LOCATION
SLOT B
PCS1002 2
RELEASED 15 SEPT 1999
INK COLOUR BLACK
TEST GEAR PIN
PRO LOGIG
BUFFER PCB
PL3
PL2
K1
K2
K4
KSZ2
PSZ1
PSZ2
E420
K469
C409
L421
K462
E406
C408
R401
R415
C411
C405
Z401
C402
C404
R407
L403
K421
K409
K467
K480
K468
K473
L416
K466
K465
C406
C410
E417
K463
D406
K464
K457
K413
K458
L401
K472
R476
R465
C453
K496
K441
K447
L402
C413
L422
C418
C421
C416
C420
C455
R419
L412
Z402
R421
K403
C419
C415
K415
K454
K445
K455
K431
K419
K470
K459
K435
C460
L407
L404
L408
C438
Z404
R431
C437
R436
K433
E4
E5
L411
R423
L405
L406
C423
RA40
C430
C427
C426
C431
K417
K491
K490
K475
C425
C452
K400
E412
K471
K428
K416
C441
K436
K437
K438
K432
K483
K402
K453
K418
K448
K439
E419
K449
L430
C496
RA50
E408
K410
K423
K442
K424
K492
E414
K422
K498
K426
C436
C440
C445
C433
C434
K456
K405
K485
K404
K451
K430
R433
L434
L431
K452
K486
K444
K434
K450
K460
K484
C446
C447
C464
C461
C465
K493
K446
K440
C448
K425
K429
K412
C463
E3
C482
C483
C478
L433
E405
E401
L425
L424
K427
D411
D405
R463
D407
E418
K488
HOLE B
LOCATION PIN

No 00025

AUDIO AMP (COMPONENT SIDE)

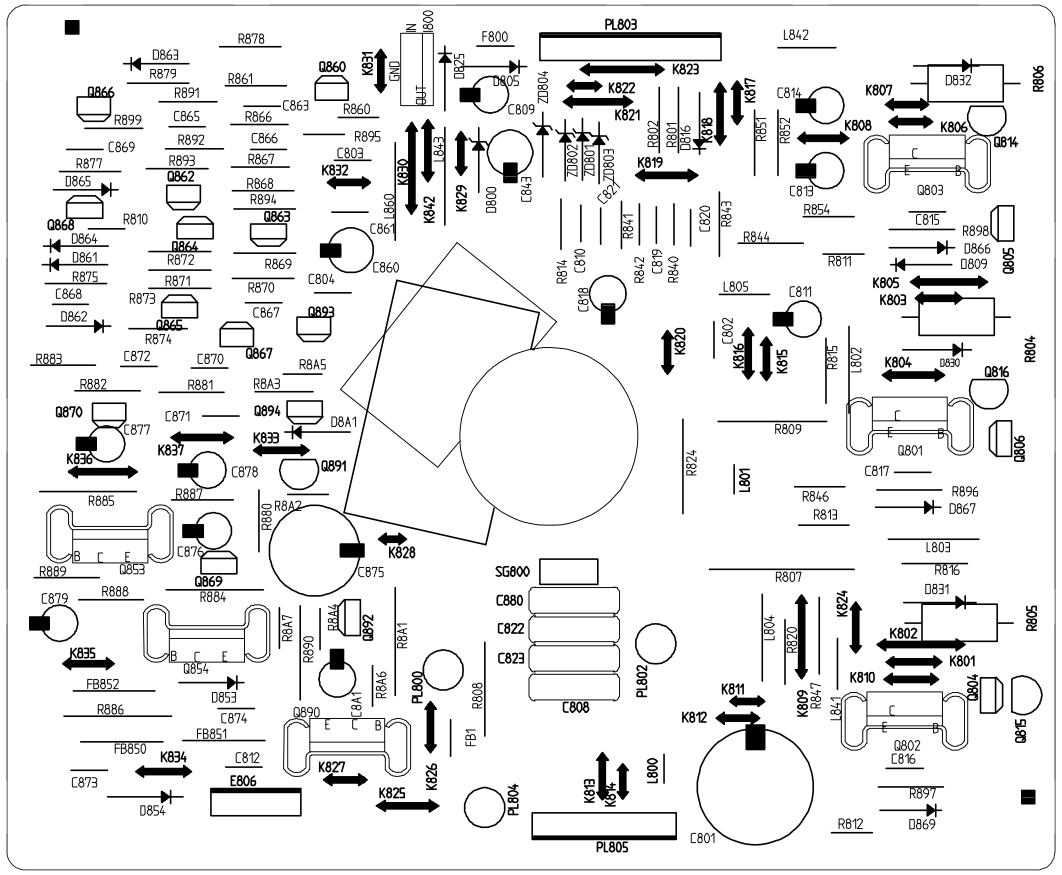
HITACHI

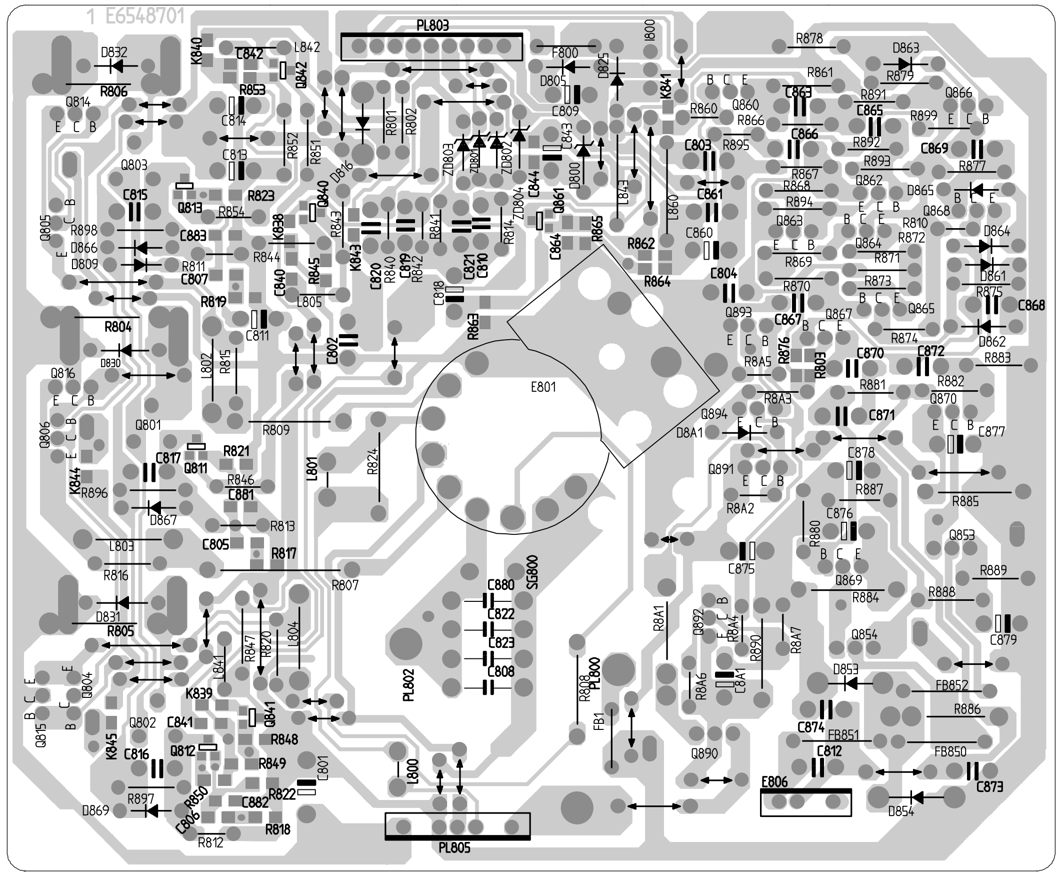

2 2 2
INK COLOUR WHITE.
SMT TARGET
DRILL TARGET
HITACHI H.E.E. LTD.
SMT TARGET
E420
C409
L421
E406
R415
C410
C406
L416
E417
R406
R426
Q412
D406
L401
C460
R442
R437
R465
R476
L407
C432
L408
Z404
L404
E4
L412
L411
L405
E41
C441
C452
C477
C431
E412
E414
K481
E401
E405
E408
E419
L430
C496
RA50
K401
DRILL TARGET
SMT TARGET
PL3
PL2
CSZ3
Z402
Q434
C420
C455
C474
C416
C421
L422
C418
R410
C429
C419
L406
C428
C472
C427
RA40
R424
C426
C430

No 00025

AUDIO AMP (SOLDER SIDE)

HITACHI

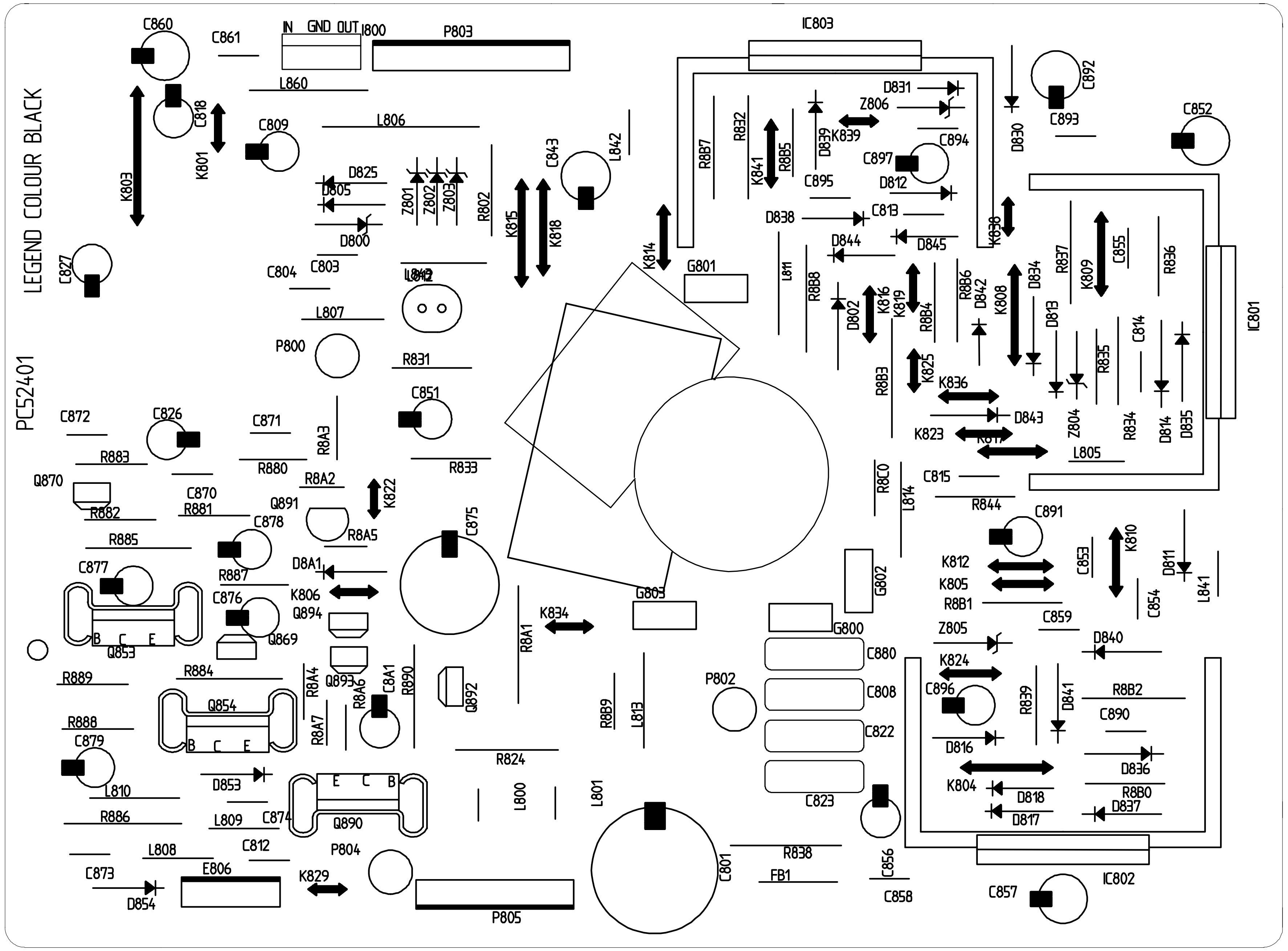

PL803
F800
L842
R878
D863
R879
R861
Q860
K831
K823
K822
K821
K817
K807
D832
R806
Q866
R891
R899
C865
C866
R895
C803
K832
K830
K842
K829
K819
R851
R852
K808
K806
Q814
Q862
Q863
Q868
Q864
Q865
Q867
Q893
Q870
Q894
K833
K836
K837
Q891
Q803
K805
K803
R844
L805
C811
Q805
K820
K816
K815
K804
Q816
Q806
Q801
R809
R824
L801
R807
SG800
C880
C822
C823
C808
K828
Q853
Q869
Q854
Q890
K835
K834
E806
K827
K825
K826
PL804
PL800
PL802
K813
L800
PL805
C801
K811
K812
K809
K810
K802
K801
K824
Q804
Q815
Q802
R812
D869
R897
D854
C873


1 E6548701
PL803
D832
K840
C842
L842
F800
R878
D863
R806
R853
Q814
R861
R879
Q866
E801
SG800
PL802
PL800
L800
PL805
E806
K839
K845
K844
R804
R805
C879
C873
D854
D869
R812
R818

No 00025

CRT 6548

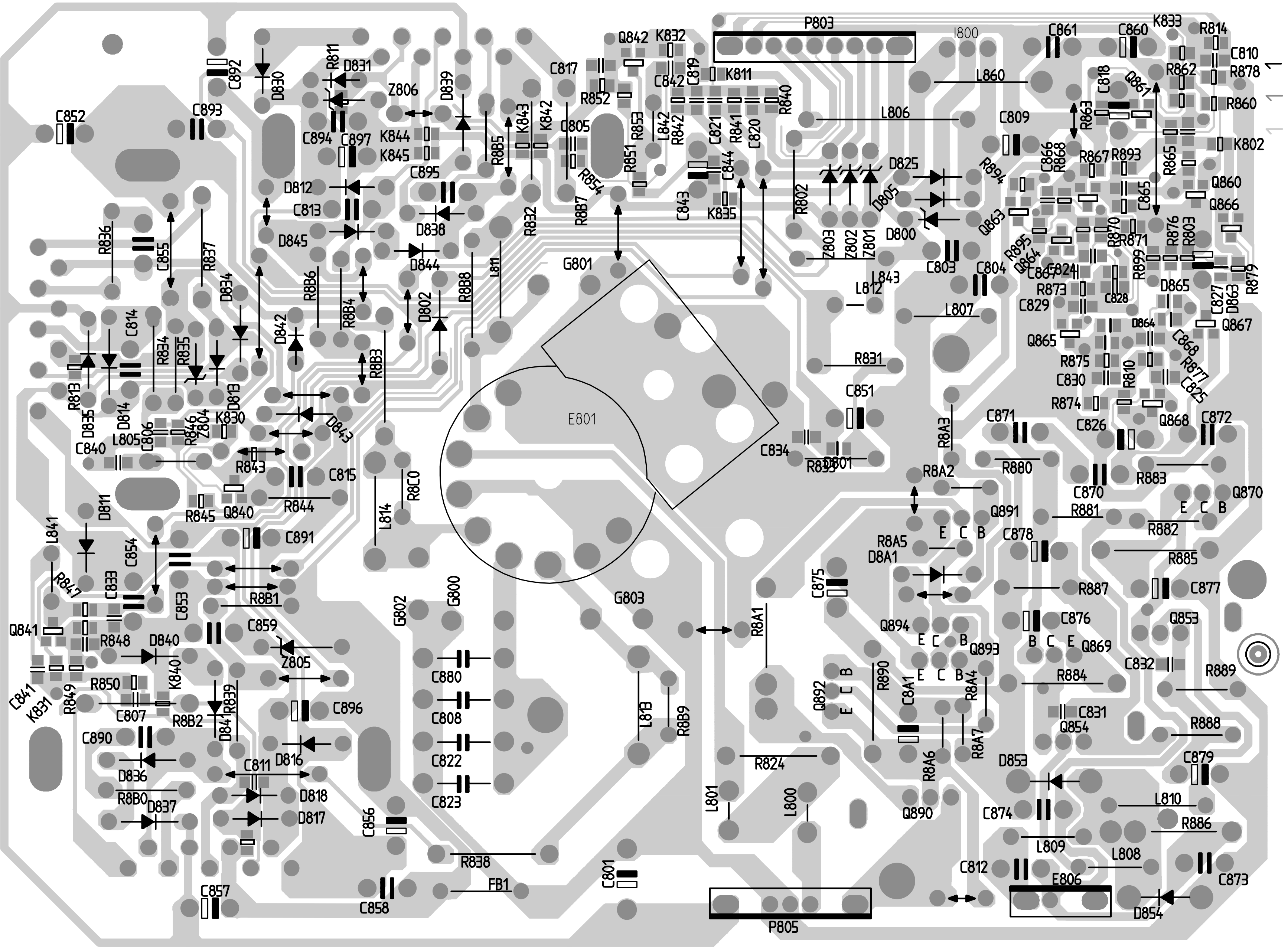
HITACHI


LEGEND COLOUR BLACK
PC52401
C860
C861
IN GND OUT
I800
P803
IC803
L860
C818
K803
K801
C809
L806
D825
D805
D800
Z801
Z802
Z803
R802
K815
K818
C843
L842
K814
G801
C804
C803
L842
L807
P800
R831
C851
C827
C872
C826
C871
R8A3
R883
R880
R833
Q870
C870
R8A2
K822
R882
R881
Q891
C878
R8A5
R885
R887
D8A1
C875
C877
C876
K806
Q894
Q869
Q853
B C E
R889
R884
R8A4
Q893
R8A6
C8A1
R890
Q892
R8A1
K834
G803
G800
P802
R888
Q854
R8A7
R889
L813
C879
R824
L810
D853
E C B
L800
L801
R886
L809
C874
Q890
L808
C812
P804
C873
E806
K829
D854
P805
C801
R838
FB1
C856
C858
C857
IC802
D831
Z806
K839
C892
C893
C852
R887
R832
K841
R885
D839
C897
C894
D830
C895
D812
D838
C813
K838
D844
D845
L811
R888
D802
K816
K819
R884
R886
D842
K808
D834
R837
K809
C855
R836
IC801
D813
C814
R835
R883
K825
K836
D843
K823
K817
Z804
R834
D814
D835
L805
R8C0
L814
C815
R844
C891
C853
K810
D811
L841
G802
K812
K805
R8B1
C854
C859
Z805
D840
C880
K824
C896
R839
D841
R8B2
C808
C890
C822
D816
D836
K804
D818
R8B0
C823
D817
D837

No 00025

CRT 524 (COMPONENT SIDE)

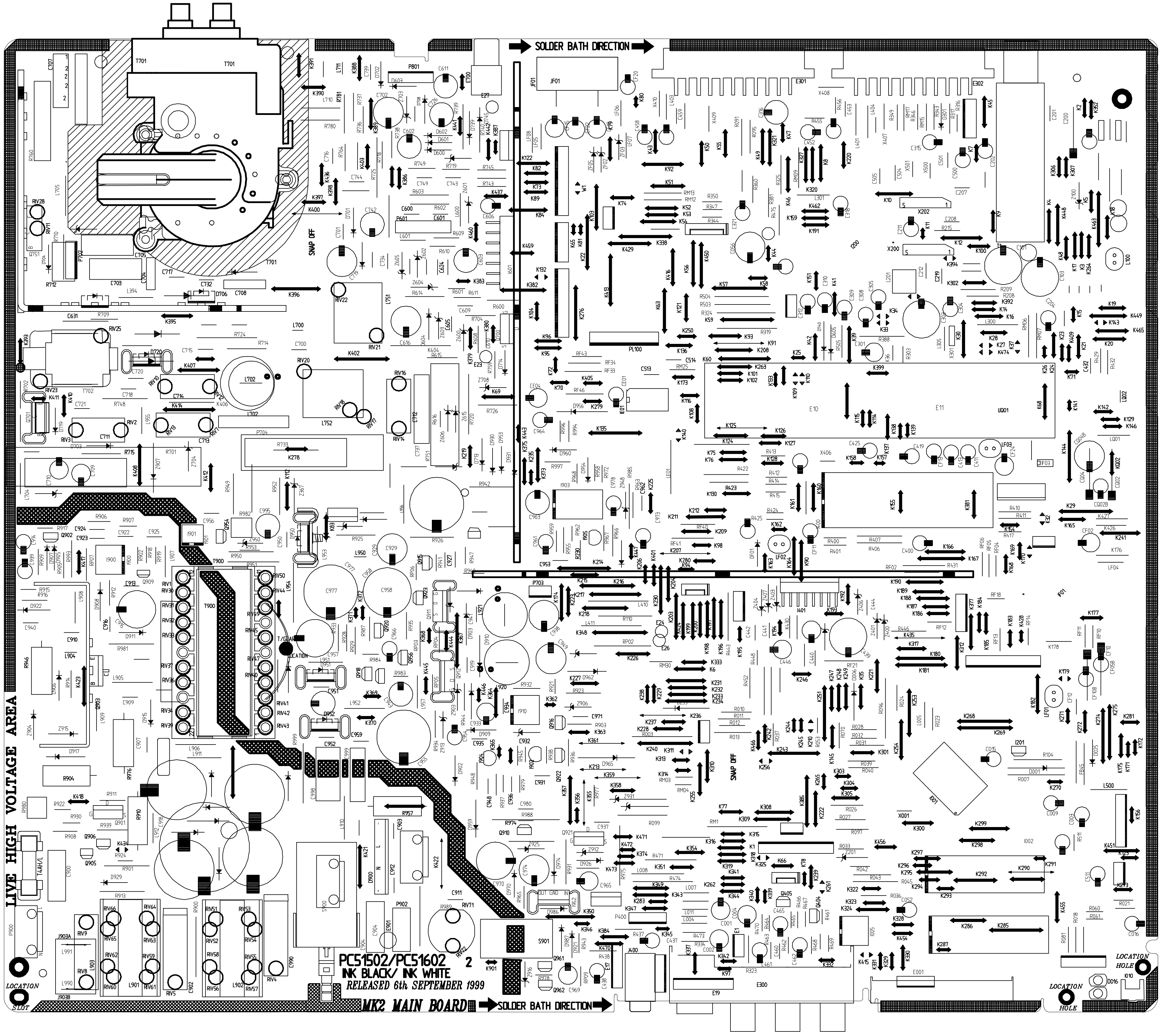
HITACHI


P803
I800
C861
C860
K833
R814
C810
R878
R860
K802
Q842
K832
K811
C819
C842
C817
R852
Q805
R851
R853
L842
R842
C821
R841
C820
R840
L860
L806
C809
C818
Q861
R862
R863
R867
R893
R865
C866
R868
Q860
Q866
C892
C893
C852
D830
R811
D831
Z806
D839
C894
C897
K844
K845
C895
R885
K843
K842
R854
C844
C843
K835
R802
D825
R894
D805
D800
Z803
Z802
Z801
Q863
C803
C804
C865
R870
R871
R876
R803
R899
R879
D865
C827
D863
Q867
R895
Q864
C824
R873
C828
C829
D864
C868
R877
C825
Q865
R875
R810
C830
R874
Q868
C872
C871
C826
D812
C813
D845
D838
D844
D802
R888
L811
R832
R887
G801
L843
L812
L807
R831
C851
C834
R833
D801
R8A3
R8A2
R880
C870
R883
Q870
R836
C855
R837
D834
D842
R886
R884
R883
C814
R834
R835
D813
D814
D835
R813
R846
Z804
K830
D843
C806
L805
C840
R843
C815
R8C0
E801
Q891
R881
E C B
R882
R8A5
C878
D8A1
R885
R887
C877
C875
C876
Q853
Q894
Q893
Q869
C832
R889
R884
C831
Q854
R888
C879
R890
Q892
C8A1
R8A4
R8A7
R8A6
D853
Q890
C874
L810
R886
L809
L808
C812
E806
C873
D854
D811
R845
Q840
R844
C891
L814
L841
R847
C854
C833
C853
R881
C859
Q841
R848
D840
Z805
G802
G800
G803
R8A1
C880
C808
C822
C823
L813
R889
R824
L801
L800
C841
K831
R849
R850
K840
C807
R8B2
D841
R839
C896
C890
C811
D816
D836
R880
D837
D818
D817
C856
R838
FB1
C801
P805
C857
C858

No 00025

CRT 524 (SOLDER SIDE)

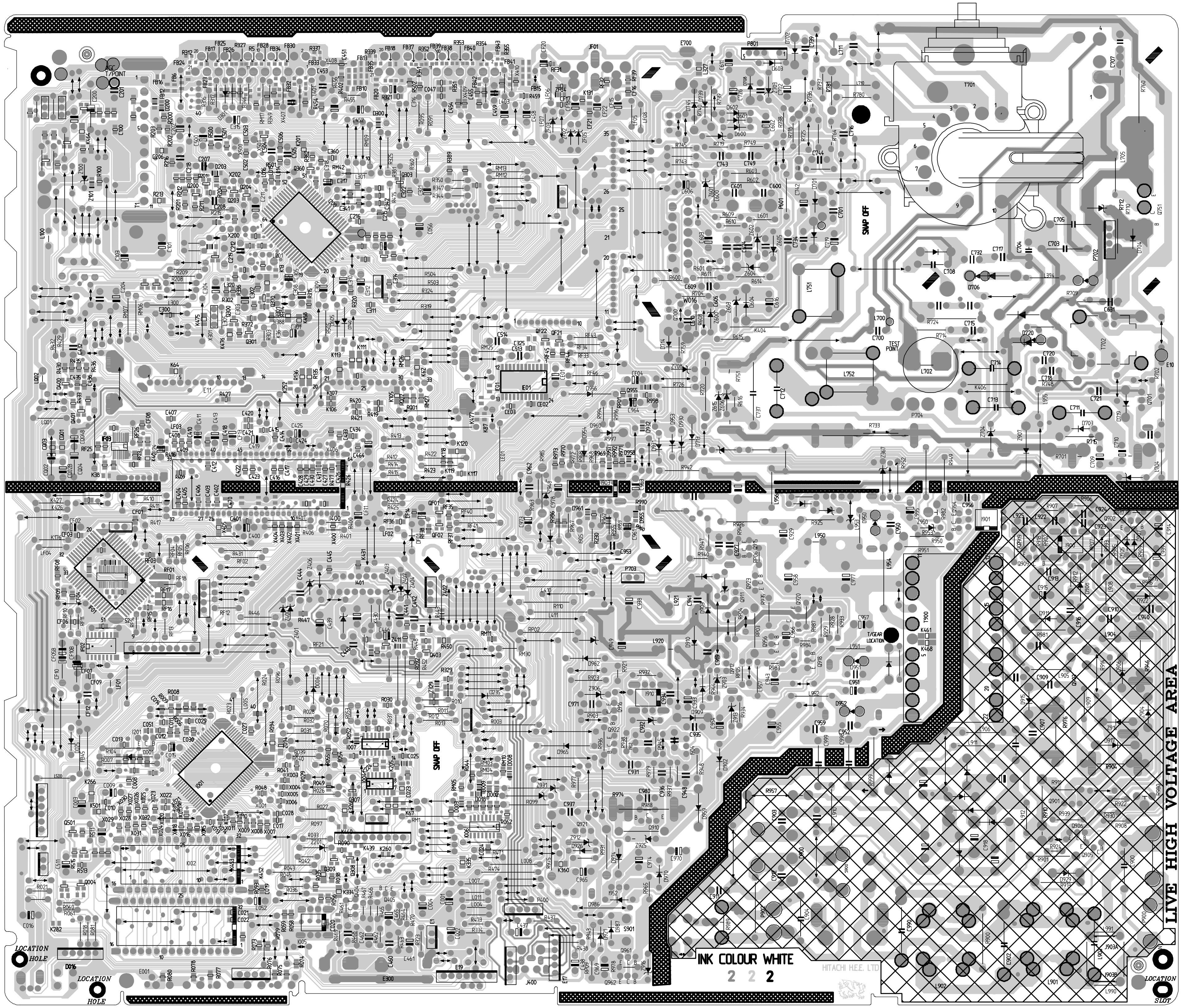
HITACHI


SOLDER BATH DIRECTION
LIVE HIGH VOLTAGE AREA
SNAP OFF
SNAP OFF
PC51502/PC51602 2
INK BLACK/ INK WHITE
RELEASED 6th SEPTEMBER 1999
MK2 MAIN BOARD
SOLDER BATH DIRECTION
LOCATION SLOT
LOCATION HOLE
LOCATION HOLE

No 00025

MAIN BOARD (COMPONENT SIDE)

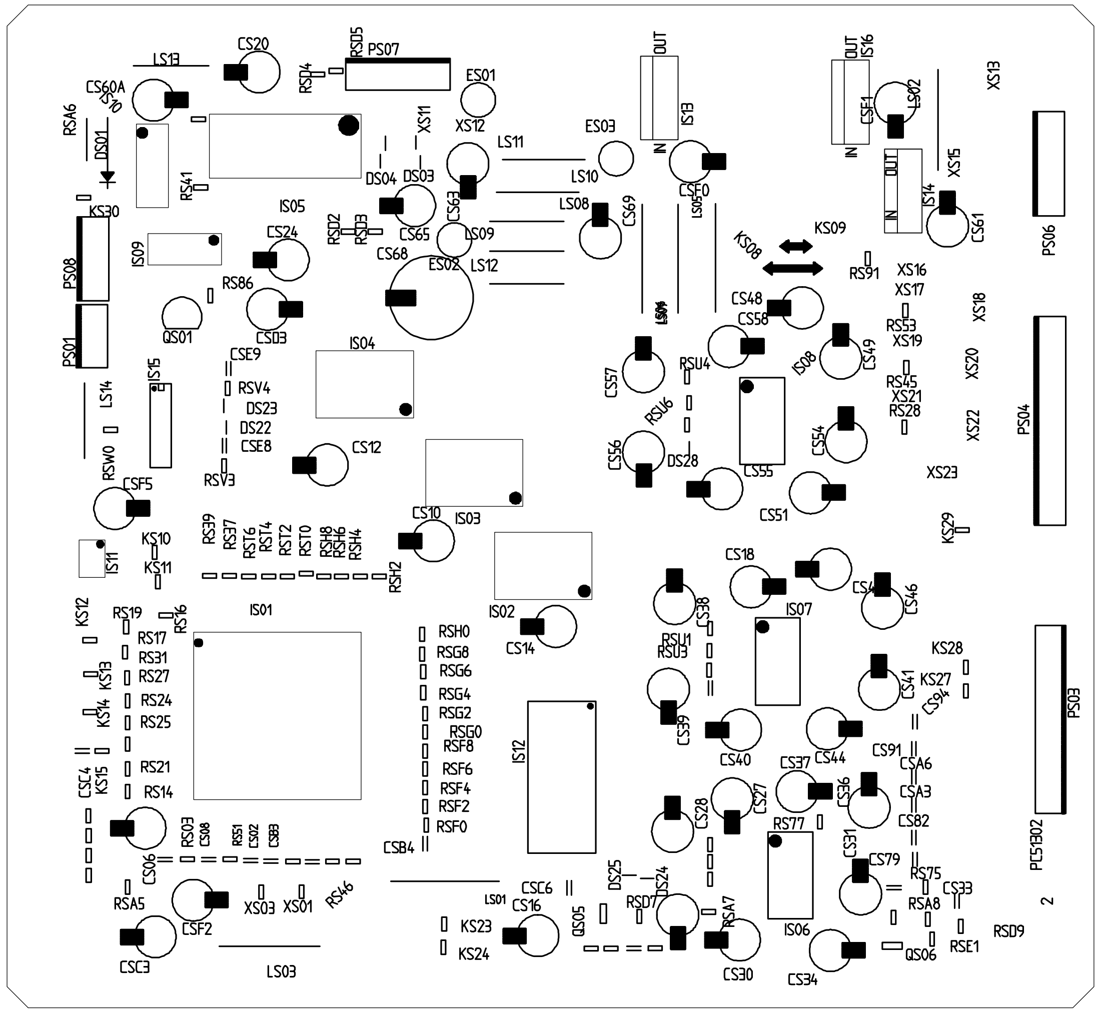
HITACHI

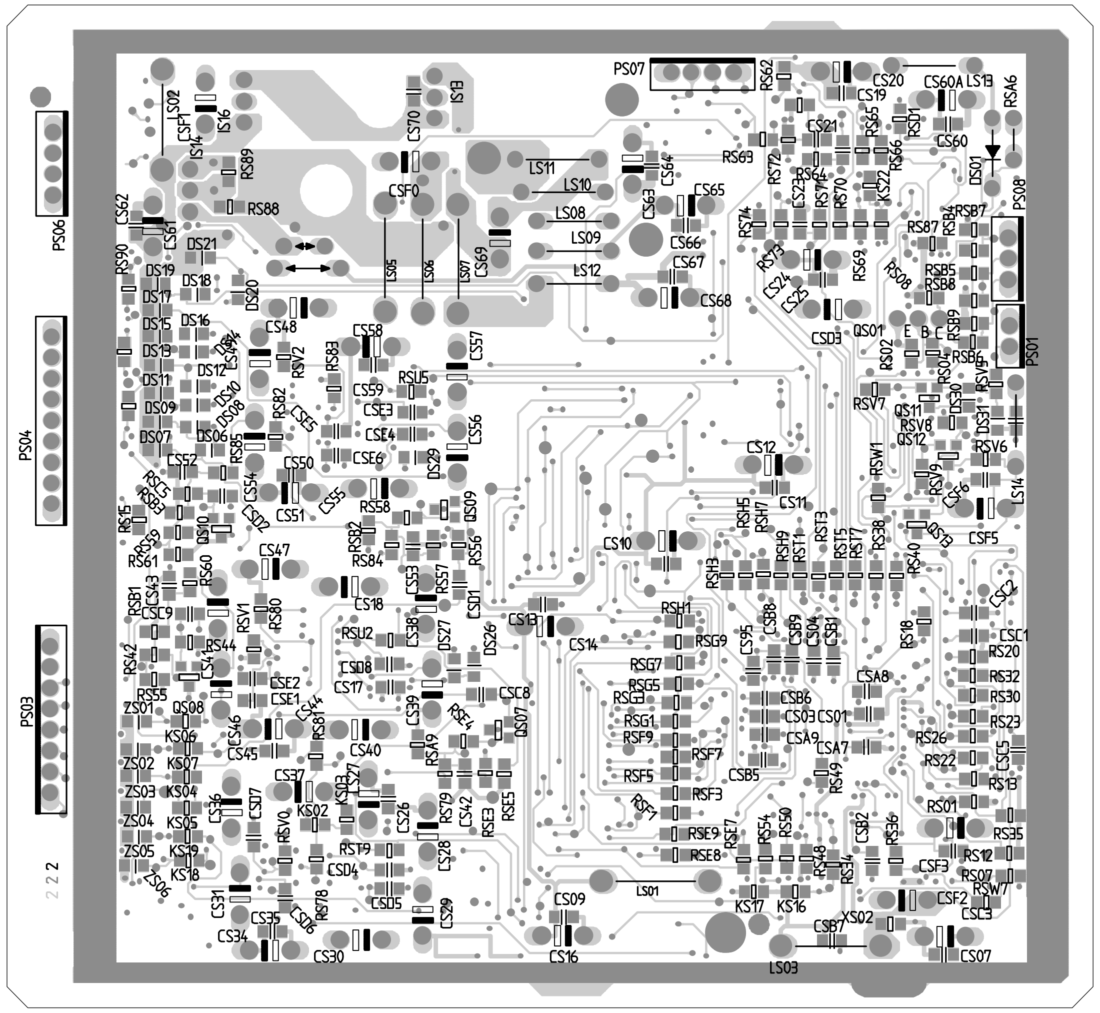

SNAP OFF
TEST POINT
INK COLOUR WHITE
LIVE HIGH VOLTAGE AREA
LOCATION HOLE
LOCATION SLOT
HITACHI H.E.E. LTD

No 00025

MAIN BOARD (SOLDER SIDE)

HITACHI

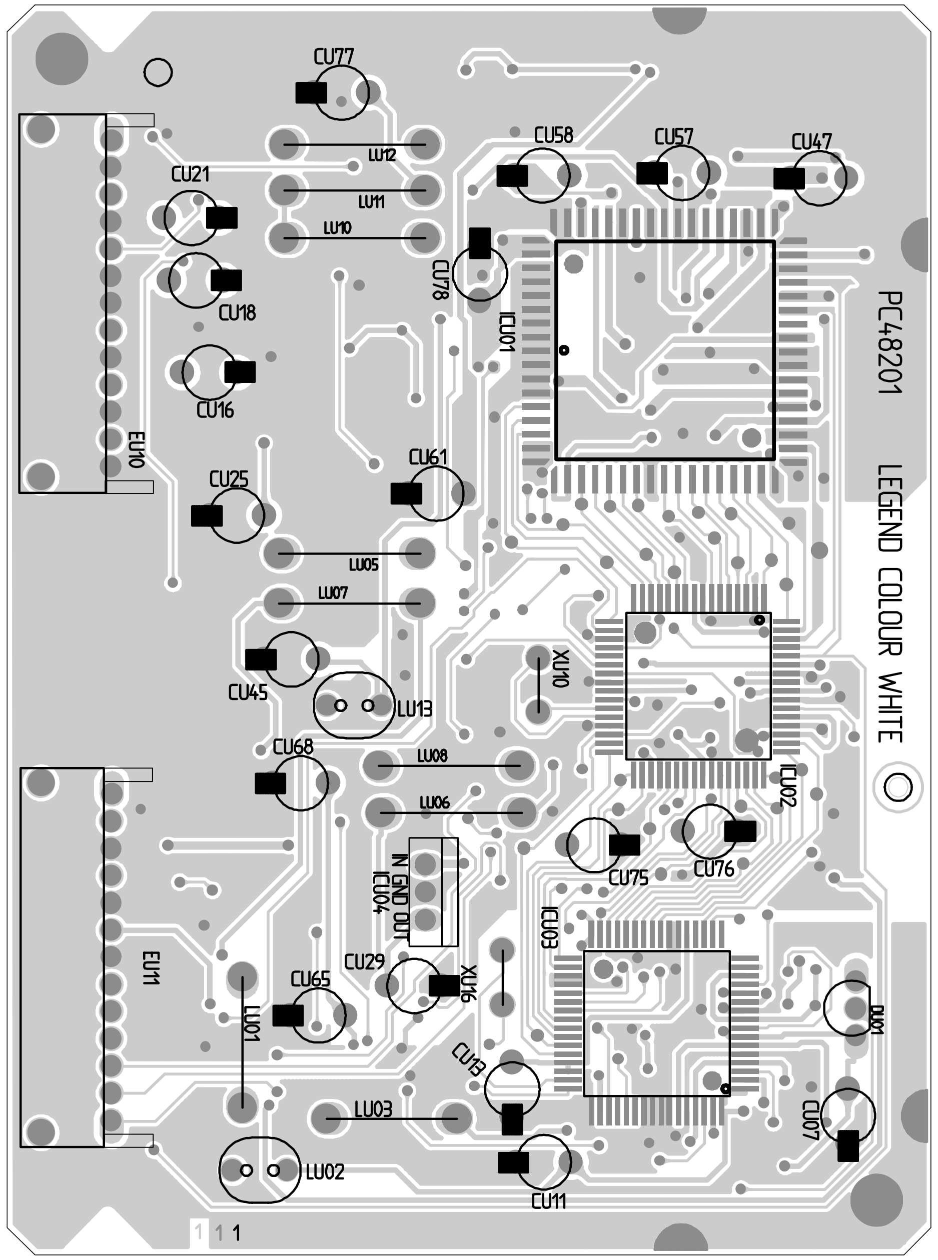

PS07
PS08
PS01
PS06
PS04
PS03
PC51302
IS01
IS02
IS03
IS04
IS05
IS06
IS07
IS08
IS09
IS12
IS13
IS14
IS16
ES01
ES02
ES03
LS03
LS08
LS09
LS10
LS11
LS12
LS13
LS14
KS08
KS09
OUT
IN
2

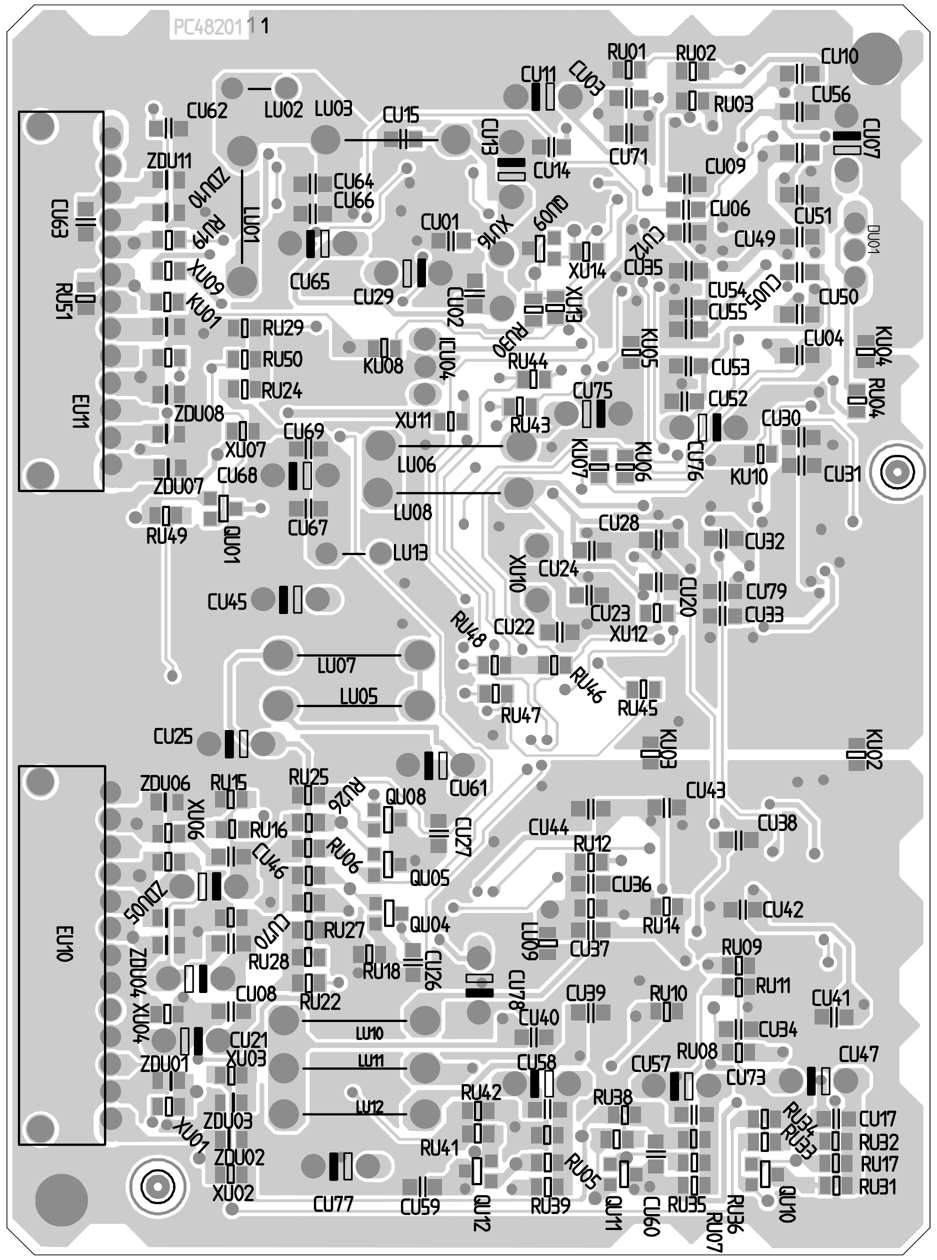

PS07
PS06
PS08
PS01
PS04
PS03
LS03
LS08
LS09
LS10
LS11
LS12
LS13
LS14
2 2 2

No 00025

DIGITAL DECODER

HITACHI

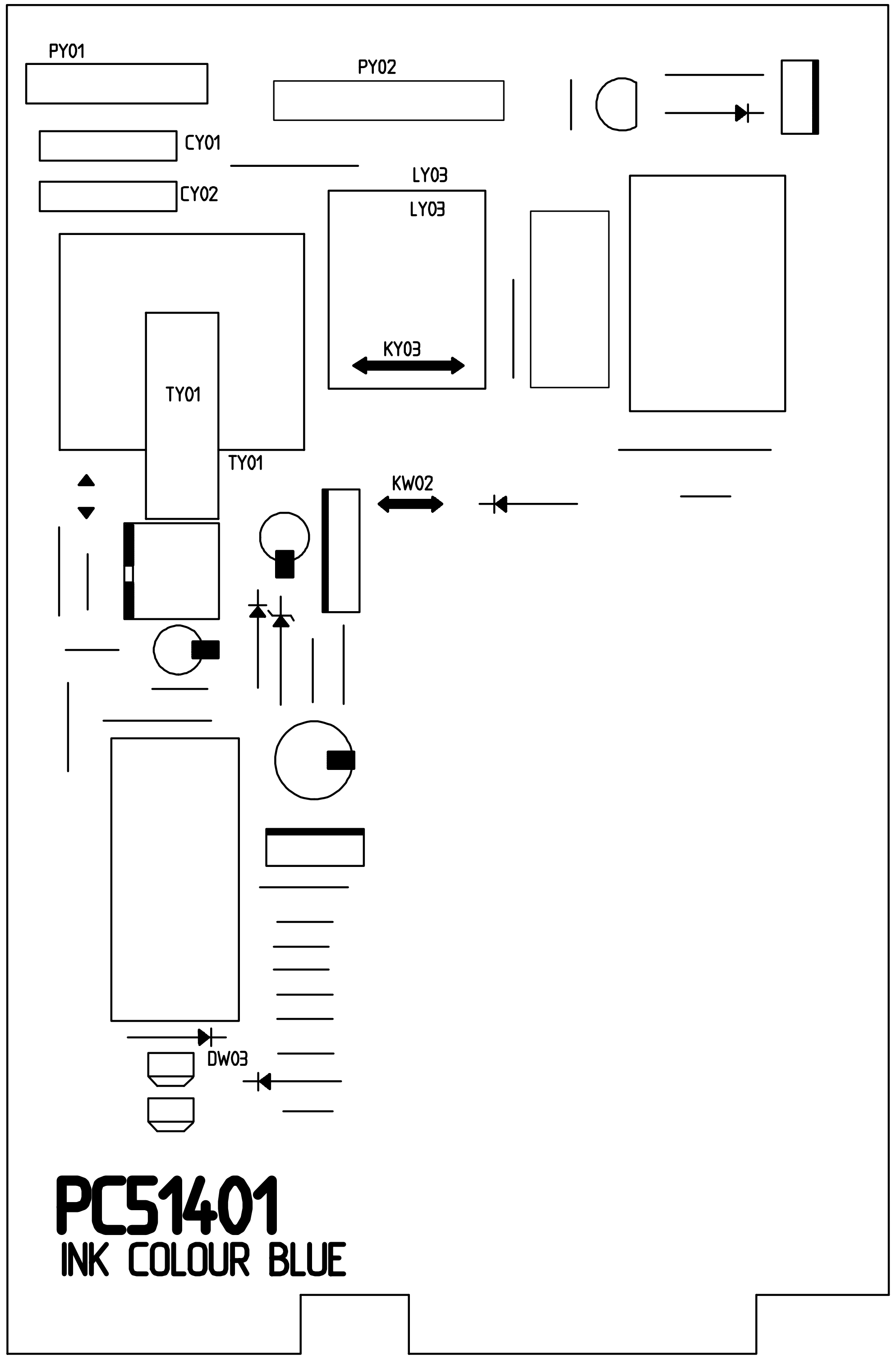

PC48201
LEGEND COLOUR WHITE
CU77
CU58
CU57
CU47
CU21
CU18
CU16
CU78
IC U01
LU12
LU11
LU10
EU10
CU25
CU61
LU05
LU07
CU45
LU13
CU68
LU08
LU06
XU10
IC U02
IC U04
IN GND OUT
CU75
CU76
IC U03
EU11
CU65
CU29
XU16
LU01
CU13
DU01
CU07
LU03
LU02
CU11
1 1 1

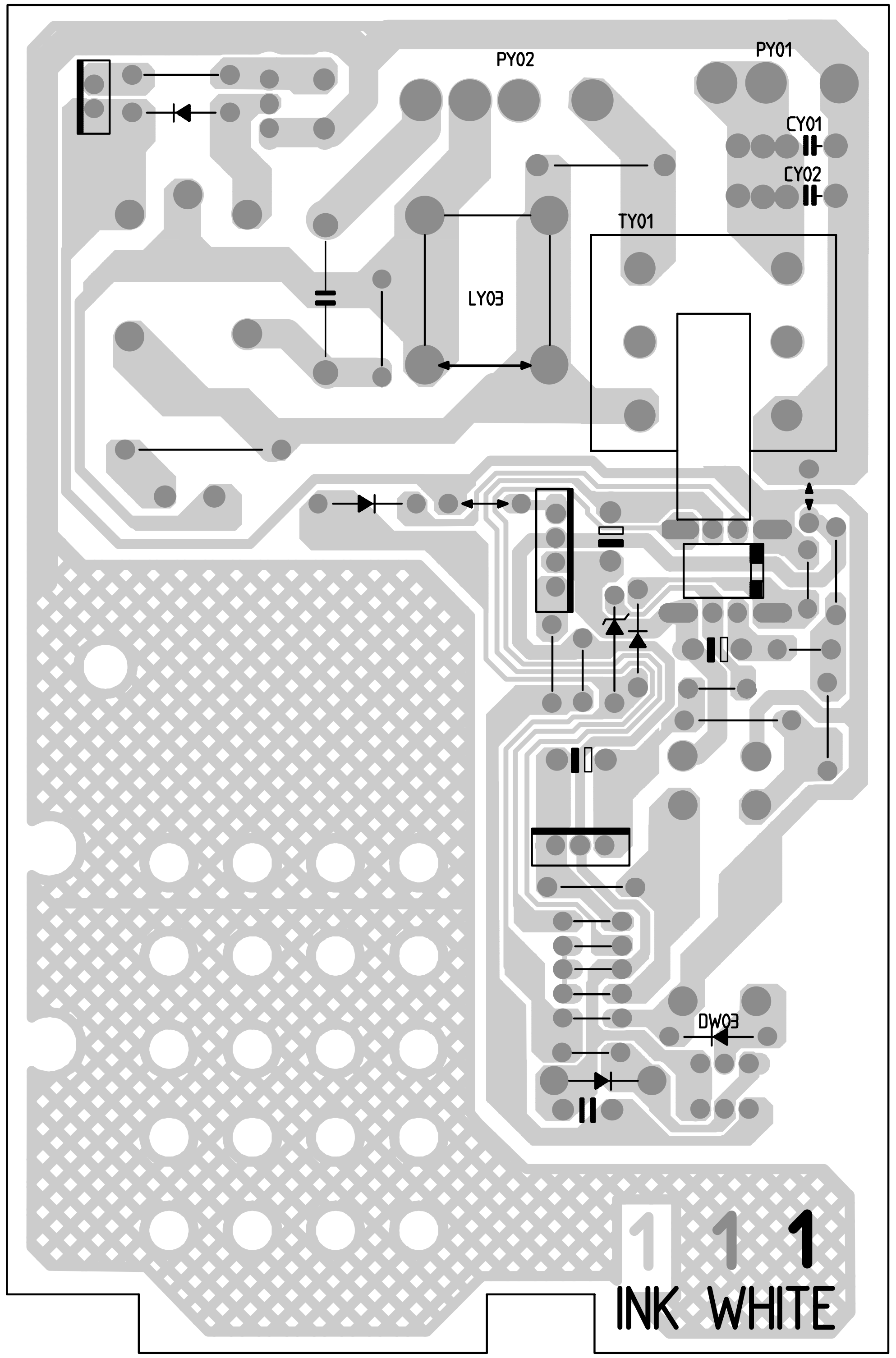

PC48201 1 1
CU62
LU02
LU03
CU15
CU11
CU03
RU01
RU02
RU03
CU10
CU56
CU07
ZDU11
CU64
CU66
CU14
CU71
CU09
CU06
CU49
CU51
CU63
RU51
CU65
CU01
CU29
CU02
XU14
CU35
CU54
CU55
CU50
RU29
RU50
RU24
KU08
RU44
CU53
CU04
KU04
RU04
ZDU08
XU11
RU43
CU75
CU52
CU30
EU11
XU07
CU69
CU68
LU06
KU10
CU31
ZDU07
RU49
QU01
CU67
LU08
CU28
LU13
CU32
CU45
CU24
CU22
CU23
XU12
CU20
CU79
CU33
RU48
LU07
LU05
RU46
RU45
RU47
CU25
KU03
KU02
ZDU06
RU15
RU25
QU08
CU61
CU43
XU06
RU16
CU46
RU06
CU27
CU44
RU12
CU38
QU05
CU36
CU42
EU10
RU27
QU04
RU14
CU37
RU09
RU28
RU18
CU26
RU11
CU08
RU22
CU39
RU10
CU41
ZDU04
XU04
LU10
CU40
CU34
CU21
XU03
LU11
CU58
RU08
CU47
ZDU01
CU57
CU73
LU12
RU42
RU38
CU17
RU32
RU17
RU31
ZDU03
RU41
ZDU02
XU02
CU77
CU59
QU12
RU39
QU11
CU60
RU35
RU36
RU07
QU10

No 00025

FEATURE BOX

HITACHI


PY01
PY02
CY01
CY02
LY03
LY03
KY03
TY01
TY01
KW02
DW03
PC51401
INK COLOUR BLUE


PY02
PY01
CY01
CY02
TY01
LY03
DW03
1 1 1
INK WHITE

No 00025

FOCUS ASSEMBLY

HITACHI

5 PARTS LIST

THE UPDATED PARTS LIST

FOR THIS MODEL IS

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